University of Manitoba
Department of Electrical & Computer Engineering

ECE 4600 Group Design Project

Final Report

Design and Implementation of an Uninterruptible Power Supply System

by

Group 03

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Abstract

Providing a steady flow of power is important for mission-critical electrical loads [1]. Slight variations in the voltage may cause these loads to fail in a way that back-up generators cannot quickly respond to. Uninterruptible power supply (UPS) systems provide a nearly instantaneous solution to these power quality problems. Designing and implementing a UPS system was the main objective of this project. Many modern UPS systems are power electronics systems composed of an online double-conversion rectifier-inverter, a battery management system, and a set of bypass systems. For this project, a half-bridge double-conversion topology was selected for its simplicity. The design topology was implemented using PLECS simulation software in order to demonstrate a proof of concept for the UPS system. As an extension of this project, additional work was done in an attempt to physically realize the system. Prototype hardware and software were developed and tested.
Contributions

Initially, there were four main components of this project: knowledge building and review of UPS systems, design, simulation, and documentation. Task leaders were assigned to individuals with collaboration often taking place. Later, we challenged ourselves to build and physical realize the UPS system. The division of labour is presented below.

<table>
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<th>Knowledge Building and Review of UPS systems</th>
<th>A. Lee</th>
<th>A. Megyeri</th>
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Acronyms

DSP – Digital Signal Processor
IGBT – Insulated-Gate Bipolar Transistor
LC – Inductor-Capacitor
LED – Light Emitting Diode
PCB – Printed Circuit Board
PI – Proportional-Integral
PWM – Pulse Width Modulation
RC – Resistor-Capacitor
RMS – Root Mean Squared
UPS – Uninterruptible Power Supply
USB – Universal Serial Bus
## Nomenclature

<table>
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<th>Term</th>
<th>Description</th>
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<tr>
<td>Bus/DC-link</td>
<td>Any graphical node of a circuit diagram where voltage, current power flow, or other quantities are to be evaluated</td>
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<td>AC</td>
<td>Alternating current waveform nature of electric power</td>
</tr>
<tr>
<td>DC</td>
<td>Direct current waveform nature of electric power</td>
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<td>DC/DC</td>
<td>DC to DC conversion</td>
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<tr>
<td>Grid</td>
<td>Power supplied by a large interconnected power system</td>
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<td>$I_{in,max}$</td>
<td>Maximum AC input current (A)</td>
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<td>$S_{rated}$</td>
<td>Rated power of the system (VA)</td>
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<td>$V_{rated}$</td>
<td>Rated AC voltage of the system (V)</td>
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<td>$V_{rms}$</td>
<td>RMS voltage (V)</td>
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<td>$V_{pk}$</td>
<td>Peak voltage (V)</td>
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<td>$V_{dc,min}$</td>
<td>Minimum DC Bus voltage (V)</td>
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<tr>
<td>$V_{out,m}$</td>
<td>Magnitude of the AC output voltage (V)</td>
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<td>Input current ripple (A)</td>
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<td>Filter inductor (H)</td>
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<td>Filter capacitor (F)</td>
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<td>$\Delta i_{L,close}$</td>
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<td>Boost converter inductor value (H)</td>
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<td>$I_{\text{inductor,avg}}$</td>
<td>Average inductor current (A)</td>
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Chapter 1 – Project Overview

A brief overview of the project is presented in this chapter including the motivation, the objectives, and the specifications.

1.1 Motivation
Providing a steady flow of power is important for mission-critical electrical loads such as data centres, life support systems, naval ships, scientific research facilities, and telecommunication systems [1]. Slight variations in the voltage may cause these loads to fail even if the power loss is only for a fraction of a second. Given the short duration of time, back-up generators cannot protect these systems. The fast response of a UPS system provides a solution to these power quality issues.

1.2 Objectives
Modern UPS systems are power electronics systems composed of a rectifier, an inverter, a battery management system, and a set of bypass systems. The ultimate goal of this project was to design and implement a UPS system in software. Specifically, our UPS system set out to rectify the grid voltage to DC voltage and invert that back to AC voltage. In addition, the system was to incorporate a back-up power supply to provide continuous power to the output for periods when the input grid voltage is unavailable.

1.3 Project Specifications
The specifications for this project were chosen to reflect real world UPS applications. We chose a power rating of 300 W to reduce the cost of components while still having useful applications. To put this power rating into perspective, 300 W is sufficient to power a single 3.9 Cu. Ft. medical refrigerator [2]. An industry standard rule-of-thumb is to plan for a power factor of 0.6 [3]. With a power factor of 0.6, 300 W is equivalent to 500 VA. Therefore, the rated power for this system is 500 VA. For simplicity, we chose to develop a single-phase system. In North America, standard single-phase power may be listed as 110 V, 115 V, 117 V, or 120 V (with some variations) [4]. We choose the standard 120 V (RMS) for our input and output rated values. Limitations on the maximum AC input current were calculated using the following equation:

\[ I_{in, max} = \frac{s_{rated}}{0.9 \cdot V_{rated}} \]  

(eq. 1-1)
Where $I_{in,max}$ is the maximum AC input current, $S_{rated}$ is the rated power of the system, and $V_{rated}$ is the rated AC voltage of the system. A 10% input voltage drop was assumed so that the maximum AC current can be found to be 4.6 A. We chose a switching frequency of 20 kHz to operate above audible frequencies as well as to decrease the size of components. In addition, we chose Insulated Gate Bipolar Transistors (IGBTs) since they can operate at these frequencies [5]. The minimum DC Bus voltage that should be maintained to prevent output voltage clipping is found using the equation:

$$V_{dc,min} \geq 2V_{out,m} = 2\sqrt{2}V_{out,rms} = 2\sqrt{2}V_{rated} \quad (eq. 1-2)$$

Where $V_{dc,min}$ is the minimum DC Bus voltage, $V_{out,m}$ is the magnitude of the AC output voltage, and $V_{out,rms}$ is the RMS of the AC output voltage. Since the value of the rated voltage is 120 V, the minimum DC Bus voltage is 340 V. The value of 380 V was chosen for the DC Bus voltage to ensure no clipping of the output sinusoidal waveform. By choosing a higher DC value, a modulation index will need to be incorporated in the waveform conversions. Table 1-1 summarizes the UPS system specifications for this project. These specifications were crucial in determining the parameters of the design topology.

<table>
<thead>
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<th>Parameter</th>
<th>Value</th>
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<th>Value</th>
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<td>120 V_{rms} (170 V_{pk})</td>
<td>Max. AC Input Current</td>
<td>4.6 A_{rms} (6.5 A_{pk})</td>
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<td>Switching Frequency</td>
<td>20 kHz</td>
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Chapter 2 – Design Topology

Our UPS design is based off of three fundamental power electronic converters; a rectifier, an inverter, and a boost converter. These three converters are connected together via a common DC Bus. In addition, our design includes two of the three main modes of operation; normal mode and battery mode [6]. The third mode is bypass mode. The next few sections describe what design topology was chosen, how they work, and why they were chosen. In addition, the analysis that was done to determine component values is presented.

2.1 Rectifier Design Topology

The rectifier design topology is based on a controlled voltage doubler rectifier consisting of an AC source, an inductor, two switching cells, and two capacitors as shown in fig. 2-1 [6]. AC voltage from the source is converted to DC voltage at the load using PWM. An inductor is placed in series with the AC source to limit the current travelling through the switching cells. In addition, each switching cell has a diode in shunt to protect the switches. The diodes will conduct when the load current cannot flow through the controlled devices. Finally, two midpoint grounded capacitors are used to maintain a steady output voltage. The advantages of using this topology are that fewer switches are required and higher DC output voltage is achieved when compared to a full bridge topology.

![Figure 2-1: A controlled voltage-doubler rectifier [6].](image)

The source side inductance of the rectifier was calculated using the equation:

\[
L_s = \frac{V_{in, min}^2}{2\Delta I_{in} P_{out} f_s} \left(1 - \frac{\sqrt{2} V_{in, min}}{V_{dc}} \right)
\]

(eq. 2-1)

Where \( L_s \) is the source side inductance, \( V_{in, min} \) is the minimum AC input voltage, \( \Delta I_{in} \) is the AC input ripple current, \( P_{out} \) is the output power, \( f_s \) is the switching frequency, and \( V_{dc} \) is the DC Bus
Design and Implementation of a UPS System

voltage. Limiting the input current ripple to 10% and setting the minimum AC input voltage to 90% of the rated value, we have:

\[ V_{in,min} = 0.9(120 \ V) = 108 \ V \]

\[ L_s = \frac{(108 \ V)^2}{2(0.1)(300 \ W)(20 \ kHz)} \left(1 - \sqrt{2}(108 \ V) \right) \left(\frac{380 \ V}{20 \ kHz}\right) = 5.8 \ mH \]

2.2 Inverter Design Topology

The inverter design topology is similar to the rectifier topology; a controlled half-bridge inverter is used as shown in fig. 2-2. In this case, the source is DC voltage and is converted to AC voltage at the load. The output filter topology is shown in fig. 2-3. An inductor is placed in series at the output of the switches to limit the current, and a capacitor is added in parallel to filter voltage harmonics. In addition, each switching cell has a diode in shunt to protect the switches. The diodes will conduct when the load current cannot flow through the controlled devices. The advantages of using this topology are similar to the rectifier topological advantages which are that fewer switches are required. However, it suffers from two inherent disadvantages [6]. The first one is poor utilization of the input DC voltage. The second one is that only bipolar PWM switching schemes can be applied with this topology. This inherently requires a larger output filter and generally leads to lower efficiency.

Figure 2-2: A controlled half-bridge inverter [6].
The PWM output from the inverter switches is filtered using an LC low-pass filter. The cut-off frequency for an LC low-pass filter is given by the following equation:

\[ f_c = \frac{1}{2\pi\sqrt{L_f C_f}} \]  \hspace{1cm} (eq. 2-2)

Where \( f_c \) is the cut-off frequency, \( L_f \) is the filter inductor, and \( C_f \) is the filter capacitor. The cut-off frequency was chosen to be 1 kHz in order to filter high order harmonics while keeping component size and cost reasonable. An inductance of 2.5 mH was selected based on a solar inverter with similar ratings [8]. From eq. 2-2, the capacitance was calculated to be 10 \( \mu \)F.

### 2.3 Boost Converter Design Topology

The boost converter design topology is based on a boost converter circuit consisting of a DC source, inductor, diode, transistor, and a capacitor as shown in fig. 2-4. Initially, the design consists of two boost converters connected in series to the DC Bus as shown in fig. 2-5. One converter maintained +190 V on the DC Bus positive line, while the other maintained -190 V on the negative line. This design minimized the potential with respect to ground of the DC Bus, as well as reduced individual component costs. However, creating the controls for the two converter design was difficult and so the single boost converter design was chosen instead.
A 24 V source represented two batteries in series. The diodes prevent current from flowing into the boost converter while the battery mode is inactive. The value of the inductor was chosen to maintain the current ripple within 20% of the inductor current. The inductor was calculated using the following equations:

\[ I_{\text{inductor,avg}} = \frac{P_{\text{out}}}{V_{\text{bat}}} \]  
\[ \Delta i_{L,p-p} = 0.2 \frac{I_{\text{inductor,avg}}}{2} \]  
\[ \Delta i_{L,\text{closed}} + \Delta i_{L,\text{open}} = \frac{V_{\text{bat}}D + (V_{\text{bat}} - V_{dc})(1-D)}{L} = 0 \]  
\[ V_{dc} = \frac{V_{\text{bat}}}{1-D} \]  
\[ L = \frac{V_{\text{bat}}D}{\Delta i_{L,p-p}f_s} \]

Where \( I_{\text{inductor,avg}} \) is the average inductor current, \( P_{\text{out}} \) is the output power, \( V_{\text{bat}} \) is the battery voltage, \( \Delta i_{L,p-p} \) is the inductor’s peak-to-peak ripple current, \( \Delta i_{L,\text{closed}} \) is the inductor current while the switch is closed, \( \Delta i_{L,\text{open}} \) is the inductor current while the switch is open, \( D \) is the duty ratio, \( V_{dc} \) is the DC Bus voltage, \( L \) is the inductance, and \( f_s \) is the switching frequency. The DC-link capacitors used in our design were calculated to have a maximum voltage ripple of 0.5%. The DC-link capacitors used in our design were calculated using the equation:

\[ \frac{\Delta V_{dc}}{V_{dc}} = \frac{1}{CRf_s} \]  

(eq. 2-8)
Design and Implementation of a UPS System

Where \( \Delta V_{dc} \) is the DC-link voltage ripple, \( V_{dc} \) is the DC Bus voltage, \( D \) is the duty ratio, \( C \) is the DC-link capacitance, \( R \) is resistance, and \( f_s \) is the switching frequency. The proposed and selected component values for the boost converter are summarized in table 2-1.

Table 2-1: Component values for the boost converters.

<table>
<thead>
<tr>
<th>Component</th>
<th>Proposed Value</th>
<th>Selected Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>( L )</td>
<td>( \geq 900 , \mu H )</td>
<td>1 mH</td>
</tr>
<tr>
<td>( C )</td>
<td>( \geq 362 , \mu F )</td>
<td>680 , \mu F</td>
</tr>
</tbody>
</table>

2.4 Normal Mode of Operation
During the normal mode of operation, power to the load is supplied continuously through the rectifier and inverter in what is known as double-conversion [6]. In double-conversion, the AC grid voltage is first converted to DC voltage and then that voltage is converted back to AC voltage at the load end. In essence, a UPS operating in normal mode produces waveforms for the load that would be equivalent to directly connecting to the grid. This mode is deactivated following a disturbance to the system.

2.5 Battery Mode of Operation
The battery mode of operation activates when the AC input voltage strays from a preset tolerance. During this mode, the battery and inverter maintain continuity of power to the load for a short duration of time. The duration of this mode is governed by the available UPS support power or whether the AC line returns within the preset tolerance.

2.6 Bypass Mode of Operation
UPS systems can be switched to bypass mode in case of internal malfunctions to the converters such as overcurrent, for fault clearing, or for maintenance. Our system is simplified and does not include bypass mode.
Chapter 3 – Controller Algorithms

A separate PWM control algorithm is used for each conversion process; rectification, inversion, and boosting. The sections of this chapter describe the PWM switching schemes used, the types of control strategies considered, and details on the control strategies used for individual converters.

3.1 PWM Switching Scheme

Our design uses the bipolar PWM switching scheme whereby a reference signal of the desired frequency is generated and compared with a high-frequency sawtooth carrier waveform [9]. The frequency of the carrier determines the switching frequency of the converter. The output of the carrier-reference comparison produces a series of pulses which are amplified by the IGBTs and filtered to reproduce a waveform at the output with the same frequency as the reference.

3.2 Open Loop Control

One simple way to control a power electronic converter would be to use open loop control. Open loop control performs the PWM switching scheme with no feedback loop. The open loop control scheme was used in this project for testing purposes because it is simple to set up.

3.3 Closed Loop Control

Closed loop control works just like open loop control except it uses feedback to regulate outputs. Various closed loop control strategies were considered for this project such as PI control, current control via hysteresis, and boundary control. Ultimately, PI control was chosen as the main technique for our system because of its simplicity.

3.3.1 The PI Controller

The PI controller served as the main control unit in this design because of its simplicity. PI controllers work to minimize the error difference between a desired reference value and the actual measured value using two control variables; the proportional gain term and the integral gain term [9]. By tuning these variables, a better response to the error can be made, and a smoother waveform will be produced.
3.4 Rectifier Control Strategy
The rectifier control strategy uses a closed loop cascaded PI control scheme to regulate the DC Bus voltage and monitor the input current. Regulation of the DC Bus is important to maintain a certain voltage level with a low voltage ripple. Monitoring the input current is important to maintain the same phase as the input voltage and to make sure it does not exceed the rated value.

3.5 Inverter Control Strategy
The inverter control strategy uses a single closed loop PI control scheme to provide a stable AC voltage waveform at the output. Monitoring the output current is also important but was not necessary for our simplified design.

3.6 Boost Converter Control Strategy
The boost converter control strategy is very similar to the rectifier strategy in that it regulates the DC Bus voltage and monitors the input current. However, in this case, the input current is monitored to protect the battery.
Chapter 4 – Implementation

Implementation of our design was done using PLECS simulation software. First, converters were simulated individually to ensure proper functionality. Then, the subsystems were combined and simulated. Throughout the simulation phase, some of the values were modified from their original design to produce better waveforms. In addition, resistive loads were used for testing purposes. Testing for reactive loads is considered beyond the scope of this project. The sections in this chapter will reflect upon the simulation outcomes; starting with the open loop inverter.

4.1 Open Loop Inverter Simulations

The open loop inverter was initially used as a stepping-stone for closed loop control schemes because of its simplicity. Closed loop control is used for the final simulations to mitigate output voltage disturbances that may occur in a real-life setting. The simulation model for the open loop inverter is shown in fig. 4-1 and the controls are shown in fig. 4-2.

![Inverter open loop circuit design](image)

**Figure 4-1:** Inverter open loop circuit design.

![Inverter open loop control scheme](image)

**Figure 4-2:** Inverter open loop control scheme.
The PWM for the open loop inverter control uses a carrier frequency of 20 kHz, and a modulation index of 0.9. The pulses from the controller are fed into the IGBT gates whereby the signal is amplified and filtered. The open loop inverter waveforms are presented in fig. 4-3. The input voltage of 380 V is converted to the rated output voltage of 120 V\text{rms} and the input current is less than the maximum specified current as stated in the specifications. The open loop inverter simulations allowed us to confirm our passive component choices and prepared us for closed loop control.

![Open loop inverter waveforms](image)

**Figure 4-3:** Open loop inverter waveforms.
4.2 Closed Loop Inverter Simulations

After testing our inverter design using open loop control, the next step was to test using closed loop control. A high-level block diagram of the inverter circuit is shown in fig. 4-4. The subsystems that make up the inverter are the source, the DC/AC converter, and the output filter as shown in fig. 4-5.

**Figure 4-4: High-level inverter circuit.**

**Figure 4-5: Closed loop inverter subsystems.**

**Figure 4-6: Inverter closed loop control scheme.**
Recall from chapter 3 that the inverter closed loop control scheme uses a single voltage feedback loop to regulate the output voltage. The DC/AC control block is shown in fig. 4-6. Using manual tuning, the PI parameters were selected and are presented in table 4-1.

Table 4-1: DC/AC PI controller parameters.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Kp1</td>
<td>0.17</td>
</tr>
<tr>
<td>Ki1</td>
<td>17000</td>
</tr>
</tbody>
</table>

With the configuration given, complementary switching pulses (S3 and S4) were generated as shown in fig. 4-7. These switching pulses were fed into the IGBT gates whereby the signal was amplified and filtered. The closed loop inverter input and output waveforms are presented in fig. 4-8. The measurements show that the DC input voltage of 380 V was converted to the AC output voltage of 120 V<sub>rms</sub> with an input current less than the maximum specified. Additional tests were done to determine the response of the closed loop control algorithm. The load was programmed to change from 50 Ω to 25 Ω at the simulation time of 0.5 seconds. The quick response of the controller is shown in fig. 4-9. With that said, the inverter simulations are satisfactory for this project and we can move on to the rectifier.
Figure 4-8: Closed loop inverter waveforms.

Figure 4-9: Inverter controller response to a change in load.
4.3 Rectifier Simulations

The rectifier control scheme can be thought of as an upgraded version of the closed loop inverter since it includes both voltage and current feedback loops. A high-level block diagram of the rectifier circuit is shown in fig 4-10 and the subsystems are in fig. 4-11. A resistance of 300 Ω was used as a load for this case. The rectifier uses a cascaded control scheme to regulate the DC Bus voltage and the AC input current. The rectifier control scheme is shown in fig 4-12.

![High-level Rectifier Circuit Diagram](image1)

![Rectifier Subsystems](image2)

![Rectifier Cascaded PI Control Scheme](image3)
The controller parameters for the rectifier were manually tuned and are presented in table 4-2.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Kp1</td>
<td>0.01</td>
</tr>
<tr>
<td>Ki1</td>
<td>33.33</td>
</tr>
<tr>
<td>Kp2</td>
<td>2</td>
</tr>
<tr>
<td>Ki2</td>
<td>5000</td>
</tr>
</tbody>
</table>

Figure 4-13: Switching pulse signals generated by the AC/DC controller.

Complementary switching pulses (S1 and S2) were generated using these parameters and are shown in fig. 4-13. These switching pulses were fed into the IGBT gates whereby the signal was amplified and stored in the DC-link capacitors. The input and output waveforms for the rectifier are shown in fig. 4-14. The DC Bus voltage was maintained at 380 V with an acceptable voltage ripple of less than 3%. In addition, the peak input current was about 6 A which is within the specified ratings.
4.4 Implementation of Normal Mode

After completing the individual inverter and rectifier simulations, the subsystem blocks were combined to implement the normal mode of operation. A high-level block diagram of the combined rectifier-inverter circuit is shown in fig. 4-15.

The AC input voltage, DC Bus voltage and AC output waveforms are shown in fig. 4-16 and the input and output currents are shown in the fig. 4-17. The peak-to-peak voltage ripple of the DC Bus is around 2% of the total voltage. The output voltage is sinusoidal with a voltage of 120 V\textsubscript{rms} as expected. Furthermore, both the input and output currents are sinusoidal and have a peak value within the rated value of 6.5 A. However, small current distortions are noticeable at the
output which may indicate problems with the filter inductor or the switching scheme. Reducing harmonic distortion is important for sensitive devices but is not within the scope of this project.

![Figure 4-16: Normal mode input, Bus, and output voltages.](image1)

![Figure 4-17: Normal mode input and output currents.](image2)
4.5 Implementation of Battery Mode

With the normal mode of operation fully functional, the next step was to implement the battery mode of operation. A major component of the battery mode yet to be tested is the boost converter. A high-level block diagram of the boost converter is shown in figure 4-18. The simulation setup was different to the original design since simulating two boost converters in series proved to be difficult. Instead, a single 24 V battery supplies a boost converter and a 300 Ω resistor as used for the load. The boost converter used in these simulations is shown in fig. 4-19.

![Boost Converter Block Diagram](image)

**Figure 4-18:** High-level boost converter block diagram.

![Boost Converter Circuit Diagram](image)

**Figure 4-19:** Boost converter circuit diagram.

In reality, battery voltage decays over time. To account for this decay, the battery was modelled with a droop setting of 0.02 V/s. This droop was subtracted from the nominal battery voltage of 24 V during the simulation. The droop battery model is shown in fig. 4-20.
Like the rectifier, the boost converter also uses cascaded PI control scheme as can be seen in fig. 4-21. The outer loop regulates the DC Bus and the inner loop controls the input current. The controller parameters for the boost converter were tuned manually. The control parameters are summarized in table 4-3.
Table 4-3: DC/DC PI controller parameters.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Kp1</td>
<td>0.1</td>
</tr>
<tr>
<td>Ki1</td>
<td>1</td>
</tr>
<tr>
<td>Kp2</td>
<td>33.33</td>
</tr>
<tr>
<td>Ki2</td>
<td>250</td>
</tr>
</tbody>
</table>

With these parameters, the DC Bus voltage was successfully regulated to the specified value of 380 V as shown in fig. 4-22. Moreover, in the steady state, the peak-to-peak voltage ripple is less than 1% and the battery current was 20 A.

Figure 4-22: DC Bus voltage regulated by boost converter.
4.6 Complete UPS System Implementation

After successfully implementing the two modes of operation, the individual subsystems were combined to form the complete UPS system. In combining the subsystems, a few challenges arose. One challenge was how to determine the mode of operation in simulation. Another challenge was resetting the PLECS PI controller blocks. The first challenge was solved by implementing a line analyser. The second challenge was solved using a customizable C-Script block. Once both these challenges were solved, the complete UPS system was implemented.

4.6.1 The Line Analyser

A line analyser was developed to determine the mode of operation. Fig. 4-23 shows a line analyser that was implemented to continuously monitor the RMS value of AC input voltage. If the value of the input voltage is below a threshold of $50 \text{ V}_{\text{rms}}$ for over 1 ms, the system switches to battery mode of operation. In doing so, the IGBTs in the AC/DC converter are disabled and disconnected from the DC Bus.

![Figure 4-23: Line analyser to monitor the input voltage.](image)

The RMS block was configured to sample the input voltage every 1 ms. After one 60 Hz period of the waveform, the number of samples can be calculated to be 17. After taking 17 samples, the RMS average of these samples is calculated and compared with $50 \text{ V}_{\text{rms}}$. The controller switches to battery mode when multiple measurements fall below the designated $50 \text{ V}_{\text{rms}}$.

4.6.2 PI Controller Reset

While a PI controller was not in use, previous values were still stored. These values needed to be reset before the controller could be reactivated. To implement the reset capability, the C-Script block was used [10]. In the C-Script block, custom code may be written on inputs. In our case, the code integrates the inputs constantly and adds it to the proportional term. Anytime the reset
input set to high, the state is reset to zero. The PLECS model and code for reset are shown in fig. 4-24 and 4-25 respectively.

![Diagram](image)

**Figure 4-24: Integrator with reset block developed in PLECS.**

**Code declarations**

```c
#define input Input(0)
#define reset Input(1)
#define output Output(0)
#define Kp ParamRealData(0, 0)
#define Ki ParamRealData(1, 0)
```

**Output function code**

```c
if (IsMajorStep)
{
    if (reset)
        ContState(0) = 0;
}

output = Kp * input + Ki * ContState(0);
```

**Derivative function code**

```c
ContDeriv(0) = input; // integrate the input
```

**Figure 4-25: Code developed for the integrator with reset.**
4.6.3 Completing the UPS System

The system was able to be implemented with the line analyser and the controller reset function. A high-level block diagram of the complete UPS system is shown in fig 4-26. The AC/DC, DC/AC, and DC/DC controllers are the same as the controllers used in individual testing except that PI with reset was used instead of the PLECS PI block. The AC/DC controller is presented in fig. 24-7 to highlight these changes.

![High-level block diagram of the complete UPS system.](image1)

Figure 4-26: High-level block diagram of the complete UPS system.

![AC/DC controller using custom PI.](image2)

Figure 4-27: AC/DC controller using custom PI.
The reset controller block is responsible for resetting the AC/DC controller when the system switches to battery mode and resetting DC/DC controller when the system switches to normal mode of operation. The reset controller block is shown in fig. 4-28.

![Diagram of reset controller block](image)

Figure 4-28: Reset function for PI controllers.

### 4.6.4 UPS System Tests

To test switching between normal mode and battery mode of operations, an amplitude modifier for the input voltage was introduced. The amplitude modifier simulates a sudden drop in input voltage which may be due to voltage sag or a power outage. The input voltage amplitude modifier is shown in fig. 4-29. In addition, the input voltage waveforms are plotted in fig. 4-30, the current waveforms are plotted in fig. 4-31, and the system voltages are plotted in fig. 4-32.

![Diagram of input voltage amplitude modifier](image)

Figure 4-29: Input voltage amplitude modifier.
Figure 4-30: Input voltages at the switching point.

Figure 4-31: Input and output currents at the switching point.

Figure 4-32: System voltages while switching from normal to battery mode.
At the simulation time of 2 seconds, the input voltage drops significantly but the output voltage is virtually unaffected staying around $120 \, V_{rms}$. This is because the line analyser sees the low value of amplitude in the input voltage and sets the battery mode flag to 1, then the AC/DC disconnects from DC Bus, and the boost converter comes into action. The entire process of correcting the output voltage takes less than two cycles. Furthermore, the DC Bus voltage returns to a steady voltage around 380 V in less than 1 second and the input current does not exceed the rated value.
Chapter 5 – Physical Realization

Following the success of our simulations, we challenged ourselves to go even further and physically realize the UPS system. The new goal was to build a prototype UPS that functioned as in our simulations. This new task consisted of three parts: hardware, software, and testing. The details on these parts and their outcomes are presented in the sections of this chapter.

5.1 Hardware

The hardware portion of our prototype consisted of a power board and a sensing board. The plan was to make a custom PCB for the power board and make the sensing circuit using bread boards.

5.1.1 The Power Board

The main hardware component developed was the power board. The power board was developed using Altium Designer software. First, individual component footprints were created, followed by the schematic diagram, and the PCB layout (see Appendix B). Furthermore, compared to the simulation models, a number of additional components were required to realize the physical UPS. Current sensors were included to provide feedback for a closed loop system. Gate driver circuits were designed to boost the switching signals going into the IGBTs. Resistive voltage dividers were used to step down high voltages so that they could be sensed without damaging the controller. Decoupling capacitors were used to maintain the DC voltage supply levels. The list of passive components used for the power board is summarized in table 5-1. In addition, a schematic of the power board is shown in fig. 5-1 and one of six gate driver schematics is shown in fig. 5-2.

Table 5-1: Passive components used for the power board.

<table>
<thead>
<tr>
<th>Component</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Voltage Dividers</td>
<td></td>
</tr>
<tr>
<td>R1</td>
<td>60 kΩ (3 x 20 kΩ)</td>
</tr>
<tr>
<td>R2</td>
<td>10 kΩ</td>
</tr>
<tr>
<td>IGBT Driver Circuit</td>
<td></td>
</tr>
<tr>
<td>R1</td>
<td>330 Ω</td>
</tr>
<tr>
<td>R2</td>
<td>330 Ω</td>
</tr>
<tr>
<td>C2</td>
<td>110 nF</td>
</tr>
<tr>
<td>C3</td>
<td>110 nF</td>
</tr>
<tr>
<td>CA</td>
<td>4.7 μF</td>
</tr>
<tr>
<td>C19</td>
<td>4.7 μF</td>
</tr>
</tbody>
</table>
Figure 5-1: Power board schematic developed using Altium.

Figure 5-2: A gate driver circuit developed using Altium.
The power board is shown in fig 5-3 fully populated and ready for testing. Jumper wires were used to make external connections to devices such as the DSP.

5.1.2 Voltage Sensing Circuits

The input, output, and DC Bus voltage sensing circuits were designed in Altium and built on a bread board using very similar circuitry. A schematic of the voltage sensing circuit is shown in fig. 5-4.

Each voltage sensing circuit is comprised of 4 stages; a voltage divider, an isolation amplifier, a differential amplifier, and a summing amplifier. A resistive voltage divider was used to step down high voltages to 200 mV as required by the selected isolation amplifier [11]. The purpose
of the isolation amplifier is to protect the controller from the high voltages present on the power board. The differential amplifier detects a difference in voltage. A summing amplifier was added during testing to offset the differential amplifier signal by 1.65 V in order for the DSP to interpret the signal correctly. The 1.65 V bias was created by dividing a 5 V source. For the dividers, three resistors in series were used to ensure greater uniformity of voltage. The equation used for voltage division is:

\[ v_o = v_i \left( \frac{R_2}{R_1 + R_2} \right) \]  
\[(\text{eq. 5-1})\]

Where \( v_o \) is the output voltage, \( v_i \) is the input voltage, \( R_1 \) and \( R_2 \) are step down resistors. The equation for the summing amplifier is:

\[ v_o = \left( 1 + \frac{Rf_2}{Rf_1} \right) \left[ v_1 \left( \frac{R_2}{R_1 + R_2} \right) + v_2 \left( \frac{R_2}{R_1 + R_2} \right) \right] \]  
\[(\text{eq. 5-2})\]

Where \( v_o \) is the output voltage, \( v_1 \) and \( v_2 \) are input voltages, \( Rf_1 \) and \( Rf_2 \) are feedback resistors, and \( R_1 \) and \( R_2 \) are input resistances. Values for differential amplifier were chosen to have unity gain. Furthermore, we chose these values for the summing amp to have gain of 1 and to produce a bias voltage of 1.65 V. The component values to realize the sensing circuit are identified in table 5-2.

### Table 5-2: Component values for the voltage sensing circuit.

<table>
<thead>
<tr>
<th>Sensing Stage</th>
<th>Component</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>High Voltage Divider</td>
<td>R1</td>
<td>990 kΩ (3 x 330 kΩ)</td>
</tr>
<tr>
<td></td>
<td>R2</td>
<td>10 kΩ</td>
</tr>
<tr>
<td>Summing Amplifier</td>
<td>Rf2 = Rf1 = R1</td>
<td>10 kΩ</td>
</tr>
<tr>
<td>Low Voltage Divider</td>
<td>R2</td>
<td>1 kΩ</td>
</tr>
<tr>
<td></td>
<td>R1</td>
<td>2 kΩ (2 x 1 kΩ)</td>
</tr>
</tbody>
</table>
5.1.3 Sensing Circuit Supply Voltages

An important consideration for this project is distinguishing between the different power sources and ground paths of the circuitry. On the voltage sensing circuit alone, there are 4 different power sources and 2 different ground paths. Two different voltages sources are required to supply the high-side transistor and the low-side transistor of the isolation amplifier. A DC/DC converter is used along with a voltage regulator to provide an isolated 5 V source for the high-side of the isolation amplifier.

Power Sources on the voltage sensing circuit are as follows:

1. High Power,
2. +5V for high-side of the isolation amplifier,
3. +5V for low-side of the isolation amplifier,
4. +15V for differential and summing amplifiers,
5. -15V for differential and summing amplifiers.

Ground Paths on the voltage sensing circuit are as follows:

1. Power Ground (voltage divider DC/DC converter and input to the isolation amplifier),
2. Signal Ground (output of the isolation amplifier, differential amplifier, summing amplifier and DSP).

Power ground is connected to the power board ground, the amplifier ground is connected to the project board ground, and the output ground is connected to the DSP ground (or signal ground) for the isolation amplifier.
5.2 Software

The software portion of physical realization focused on producing switching pulse for the IGBTs and obtaining the desired waveforms. Lab-Volt equipment was used to help realize the software. The details included in this section are on the controller development, the controller algorithm development, and the inverter tests that were done.

5.2.1 Controller Development

A DSP was used to generate switching pulses for the IGBTs because it is easier than their analog counterparts. Initially, the 90 MHz F28069 Piccolo developed by Texas Instruments was selected for its PWM capabilities [12]. Later, the controller was changed to the 150 MHz TMS320F28335 because it was faster and had lower power consumption rating [13]. Furthermore, a docking station with a USB connection was used to program the device. With a functioning controller, tests were done to interface and learn how the controller could be used. The first test was to interface with an LED. Following the success of that program, a simple open loop buck converter algorithm was developed to see if we could utilize the built-in PWM schemes. The Lab-Volt IGBT block was used to help realize the algorithm. The Lab-Volt test setup for the open loop buck converter is shown in fig. 5-5.

Figure 5-5: Test setup for the open loop buck converter.
Fig. 5-6 shows the input and output voltages for the buck converter setup using a duty ratio of 50%. Although the results were not as expected, the important thing is that we were able to interface the DSP with hardware.

5.2.2 Controller Algorithm Development

During the controller development, we learned a fast way to program the DSP using MATLAB/Simulink. Using the controller algorithms developed in PLECS, control block diagrams were created in MATLAB/Simulink, and then converted to code. The programming method is presented in Fig. 5-7. The only challenge was to properly configure the Simulink blocks.

- a) Simulations are done in PLECS.
- b) PLECS blocks are remodeled in MATLAB/Simulink.
- c) MATLAB converts the blocks into C code.
- d) Pins are connected and the program is run.

Figure 5-7: Software programming method.
There were two main blocks that needed to be configured in Simulink; the ePWM block and the ADC block. The ePWM block produces an output pulse given a number of parameters. The Lab-Volt IGBTs we planned to use were rated for 10 kHz. Thus, the ePWM was configured to generate a 10 kHz sawtooth. In addition, a dead band period of 200 cycles was incorporated to protect the IGBTs. For the 150 MHz controller, 200 cycles is approximately 1.33 μs. Using an oscilloscope, the dead band was measured to be 1.4 μs as shown in fig. 5-8.

![Figure 5-8: Dead band time programmed for switching.](image)

The ADC block was configured based on the TMS320F28335 data sheet [12]. The equations used for the ADC is shown in fig. 5-9. The ADCLO term was assumed zero.

<table>
<thead>
<tr>
<th>Digital Value</th>
<th>Equation</th>
<th>Condition</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>$4096 \times \frac{\text{Input Analog Voltage} - \text{ADCLO}}{3}$</td>
<td>$0 \leq \text{Input} &lt; 3 \text{ V}$</td>
</tr>
<tr>
<td>4095</td>
<td></td>
<td>$\text{Input} \geq 3 \text{ V}$</td>
</tr>
</tbody>
</table>

![Figure 5-9: Analog-to-Digital Converter Module for the TMS320F28335 [12].](image)
5.3 Testing

After learning some of the capabilities of the controller, we applied those teachings to our UPS application. The first and only tests completed were for a low voltage inverter. The two tests performed were open loop control, and closed loop control.

5.3.1 Open Loop Inverter Test

The open loop control was programmed by pulse width modulating a discrete sine wave block in Simulink. Since time and money were limited we utilized readily available components from the lab and the electrical shop to make prototype test circuits. Lab-Volt equipment was used for the DC input voltage source and the IGBT module. A 20 mH reactor rated for 10 A was used as the series inductance. Two 680 µF electrolytic capacitors rated for 35 V were used as the DC-link capacitors. A 30 Ω resistor was used for the load. The input voltage and current for the open loop inverter test are shown in fig. 5-10. The output voltage waveform is shown with pink and blue switching pulses in fig. 5-11.

![Figure 5-10: Input voltage and current for the open loop inverter test.](image1)

![Figure 5-11: Output voltage waveform for the open loop inverter test.](image2)
The inversion process was successful for the open loop inverter. However, the output voltage amplitude was not as high as expected. We concluded that a closed loop control was necessary to regulate the output voltage.

5.3.2 Closed Loop Inverter Test

The closed loop inverter required at least one voltage feedback according to our simulations. Thus, a prototype voltage sensing circuit was developed on a power board using available electrical components. The sensing circuit is shown on the power board in fig. 5-12 and the closed loop inverter test setup is shown in fig. 5-13.

Figure 5-12: Prototype sensing circuit.

Figure 5-13: Closed loop inverter test setup.
In addition, the same component values used in the open loop inverter were used for the closed loop inverter. The goal of this setup was to obtain a 12 V\textsubscript{rms} (17 V\textsubscript{pk}) waveform from a 40 V DC input as a low voltage equivalent of our simulations. Controller parameters were tuned until the correct waveform was obtained. The control block diagram used is shown in fig. 5-14. A summary of the parameter values used are presented in table 5-3.

![Block diagram](image)

**Figure 5-14:** Control block diagram for the closed loop inverter.

**Table 5-3:** Closed loop inverter control.

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The input of the closed loop inverter is shown in fig. 5-15. Furthermore, the output and switching pulses are shown in fig 5-16.

![Input voltage and current for the closed loop inverter test.](image1)

Figure 5-15: Input voltage and current for the closed loop inverter test.

![Output voltage for the closed loop inverter test.](image2)

Figure 5-16: Output voltage for the closed loop inverter test.

The figure shows an output waveform of 17 V\(_{\text{pk}}\) as expected. Some small distortions in the waveform appear which may be caused by using improper component values. Other sources of distortion were found during testing. For example, the voltage waveform was clipped when incorrect bias values were used. In the future, reducing harmonic distortion will be important for developing a good quality UPS system.
Chapter 6 – Conclusions

Motivated by the power quality issues faced in industry, the design and implementation of a UPS system was the goal of this project. The outcomes of the project and possible future work are discussed in this chapter.

6.1 Project Outcomes

This project met and exceeded expectations. A single phase 500 VA UPS system was designed and implemented. In particular, a double-conversion rectifier-inverter topology was designed and implemented using PLECS simulation software. In addition, a boost converter, a line analyser and an amplitude modifier were developed to implement the battery mode. Subsystems were tested separately and then combined. The input and output voltage waveforms of the combined system was 120 V with an input below 4.6 A as specified. Following the success of our system, we challenged ourselves to physically realize the system. Hardware and software were developed to realize the system. A closed loop inverter was tested and realized. The allocated budget for this project was $400.00 and our final budget was $299.03 (see appendix A). We would like to thank our advisor for all the help and support he’s provided for us in the past year. All four of us had a very positive experience and we learned a lot about project management and engineering design.

6.2 Future Work

The present implementation has met the required specification. However, we recognize that there are a number of areas which can be expanded upon. First and foremost would be to perform low voltage tests. The hardware components purchased for this project can be reused for future work in physical realization. Second would be the development of a high voltage safe case to test at the specified high voltages. This development would include incorporating a battery management system, and implementing bypass mode. The PI control scheme may also be changed to other controllers which have faster response such as a hysteresis controller or a boundary controller. Many other developments exist such as using EMI filters at the inverter output to make the device more immune to electromagnetic interference, modifying and expanding to a 3-phase system, designing a system for higher power ratings, reducing harmonic distortion, or improving efficiency.
References


Appendix A – Budget

Table A-1 below summarize the project budget for material and capital expenditures used in our project. As a group of four students, we have generously been awarded the sum of $400.00 by the University of Manitoba's Electrical and Computer Engineering Department to be used for project expenditures. The total cost of our project exceeded the awarded budget. However, additional costs were generously covered by our faculty advisor.

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Appendix B – Additional Hardware

Figure B-1: PCB layout.
Figure B-2: Voltage sensing circuit for a closed loop rectifier.