Design and Implementation of a Variable-Frequency Drive Using a Multilevel Topology

by

Group 03

Kale Ewasiuk
Curtis Shumski
Edwin Ifionu
Matthew Szyda

Final report submitted in partial satisfaction of the requirements for the degree of Bachelor of Science in Electrical and Computer Engineering in the Faculty of Engineering of the University of Manitoba

Academic Supervisor
Dr. Shaahin Filizadeh - University of Manitoba

Industry Supervisor
Steven Howell - Manitoba Hydro

Internal Supervisor
Carl Ho - University of Manitoba

Date of Submission
March 4, 2015
Abstract

This report describes the development of a variable-frequency drive using a multilevel topology. Modern electrical systems are increasingly relying on high-performance power electronic equipment to improve efficiency, quality, and controllability. Modular Multilevel Converters (MMC) are a growing breed of voltage source converters (VSC) used in high voltage applications such as power transmission and motor drives. The (MMC) was the chosen topology because it provides better performance compared to conventional 2-level VSCs in exchange for more complex control schemes. The main objective of this project was to design and manufacture a single-phase prototype of the MMC. This report discusses simulation results that confirmed that a single-phase prototype of the MMC can be realized with the designed control schemes. A cascaded half-bridge sub-module prototype was manufactured and tested which demonstrated a proof of concept. PCB sub-module designs were implemented to aid in the manufacture of the converter. The single-phase converter was designed to drive a fixed resistive-inductive load of 100VA with the specification of producing low output voltage harmonic distortion. This report demonstrates the integration of MMC sub-systems that are required to build a single-phase prototype.
## Contributions

<table>
<thead>
<tr>
<th>Task</th>
<th>Kale Ewasiuk</th>
<th>Edwin Ilion</th>
<th>Curtis Shumski</th>
<th>Matthew Szyda</th>
</tr>
</thead>
<tbody>
<tr>
<td>Research</td>
<td>o</td>
<td>o</td>
<td>o</td>
<td>o</td>
</tr>
<tr>
<td>Main Component Selection</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Simulation</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Switch and Gate Driver Circuitry</td>
<td>o</td>
<td></td>
<td></td>
<td>o</td>
</tr>
<tr>
<td>Reference and Modulation Control</td>
<td></td>
<td>o</td>
<td>o</td>
<td></td>
</tr>
<tr>
<td>Capacitor Voltage Balancing and Sub-Module Sorting</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Voltage Measurement System</td>
<td>o</td>
<td></td>
<td>o</td>
<td>o</td>
</tr>
<tr>
<td>Current Direction Measurement System</td>
<td></td>
<td></td>
<td></td>
<td>o</td>
</tr>
<tr>
<td>User Interface</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Starting Routine</td>
<td></td>
<td>o</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Capacitor Discharge System</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>PCB Design and Fabrication</td>
<td>o</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Legend:  ● Lead task  ○ Contributed
Acknowledgements

We would like to thank a number of people, without whom this project could not have been complete. First and foremost we would like to thank our academic supervisor Dr. Shaahin Filizadeh for his guidance and expertise. We would also like to thank our industry supervisor Mr. Steven Howell for his advice and assistance.

Additionally we would like to thank Dr. Behzad Kordi for his feedback on our coursework, Mr. Dan Card for his guidance and feedback on circuit design and engineering philosophy, and Ms. Aidan Topping for the constructive feedback on our coursework.

Dr. Ken Ferens for providing us with the microcontrollers, Mr. Glen Kolansky for his help and advice, Mr. Sinisa Janjic for helping with the soldering, Mr. Zoran Trajkoski for the manufacturing of the PCBs and help with soldering and Mr. Erwin Dirks for fabricating the housing unit.

Finally, we would like to thank our families and friends for their support throughout the project and our university education.
# Table of Contents

Abstract ......................................................... i
Contributions ................................................... ii
Acknowledgements .............................................. iii
List of Figures .................................................. viii
List of Tables .................................................. xi
Nomenclature ................................................... xii

1 Introduction .................................................. 1
   1.1 Motivation ............................................... 1
   1.2 Project Objectives ....................................... 2
   1.3 Project Specifications ................................... 2

2 Background ................................................... 4
   2.1 Converter Topology ....................................... 4
   2.2 Half-Bridge Sub-Modules ................................ 5
   2.3 Basic Converter Analysis ................................ 7
   2.4 Converter Control ....................................... 11
      2.4.1 Nearest Level Control ............................. 11
      2.4.2 Pulse-Width Modulation ........................... 13
      2.4.3 Level-Shifted Carrier Pulse Width Modulation . 13

3 Preliminary Converter Design ............................... 15
3.1 Component Selection ........................................ 15
   3.1.1 Sub-Module Capacitor Selection ......................... 16
   3.1.2 Arm Inductor Selection ................................ 16
   3.1.3 Capacitor and Inductor Finalization .................... 17
   3.1.4 Future Design Flexibility ............................... 19
3.2 Simulation ................................................... 20
   3.2.1 MMC Modelling ......................................... 20
   3.2.2 Simulation Parameters .................................. 23
   3.2.3 Simulation Results ..................................... 23

4 MMC Sub-Systems .............................................. 28
   4.1 Switch and Gate Driver Circuitry ......................... 29
      4.1.1 Switches ............................................. 30
      4.1.2 Gate Driver Integrated Circuit ....................... 30
      4.1.3 Optocoupler .......................................... 31
      4.1.4 Dead-Time Generator ................................. 31
      4.1.5 Gate Driver Implementation ............................ 32
   4.2 Reference and Modulation Control ......................... 35
      4.2.1 Implementation ....................................... 35
   4.3 Capacitor Voltage Balancing and Sub-Module Sorting .... 40
      4.3.1 Balancing Algorithm .................................. 41
      4.3.2 Bubble Sort ........................................... 41
      4.3.3 Quick Sort ............................................ 42
      4.3.4 Methodology .......................................... 45
      4.3.5 Optimizing the Algorithm ............................ 46
   4.4 Voltage Measurement System ............................... 47
      4.4.1 Voltage Measurement System Design .................... 47
<table>
<thead>
<tr>
<th>Section</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>4.4.2 Analog-Digital Converter</td>
<td>50</td>
</tr>
<tr>
<td>4.4.3 Multiplexer</td>
<td>51</td>
</tr>
<tr>
<td>4.5 Current Direction Measurement System</td>
<td>52</td>
</tr>
<tr>
<td>4.6 User Interface</td>
<td>54</td>
</tr>
<tr>
<td>4.6.1 Keypad</td>
<td>54</td>
</tr>
<tr>
<td>4.6.2 Liquid Crystal Display</td>
<td>55</td>
</tr>
<tr>
<td>4.7 Starting Routine</td>
<td>58</td>
</tr>
<tr>
<td>4.8 Capacitor Discharge System</td>
<td>59</td>
</tr>
<tr>
<td>4.9 Printed Circuit Board Design and Fabrication</td>
<td>61</td>
</tr>
<tr>
<td>4.9.1 General PCB Considerations</td>
<td>62</td>
</tr>
<tr>
<td>4.9.2 Sub-Module PCB</td>
<td>62</td>
</tr>
<tr>
<td>4.9.3 Data Distribution PCB</td>
<td>62</td>
</tr>
<tr>
<td>4.9.4 DC-Link PCB</td>
<td>63</td>
</tr>
<tr>
<td>4.9.5 Current Direction Measurement PCB</td>
<td>63</td>
</tr>
<tr>
<td>4.9.6 PCB Fabrication</td>
<td>63</td>
</tr>
<tr>
<td>5 System Integration Testing</td>
<td>65</td>
</tr>
<tr>
<td>5.1 Gate Driver Testing</td>
<td>65</td>
</tr>
<tr>
<td>5.2 Microcontroller Testing</td>
<td>66</td>
</tr>
<tr>
<td>5.3 Current Direction Measurement Testing</td>
<td>67</td>
</tr>
<tr>
<td>5.4 Converter Arm Testing</td>
<td>68</td>
</tr>
<tr>
<td>6 Future Work</td>
<td>72</td>
</tr>
<tr>
<td>6.1 Switch Protection</td>
<td>72</td>
</tr>
<tr>
<td>6.2 Proposed Gate Driver Revision</td>
<td>72</td>
</tr>
<tr>
<td>6.2.1 Three-phase Converter</td>
<td>74</td>
</tr>
<tr>
<td>6.2.2 Closed-loop Converter Control</td>
<td>74</td>
</tr>
</tbody>
</table>
7 Conclusions ................................................................. 75

References ................................................................. 77

Appendix A Printed Circuit Board Layouts .............................. 80

Appendix B Budget .......................................................... 85

Appendix C Second Appendix ............................................. 87

C.1 Master Microcontroller Functions ................................. 87
  C.1.1 Main Function ................................................... 87
  C.1.2 Device Initialize ............................................... 87
  C.1.3 Interrupt initialization ....................................... 87
  C.1.4 Timer2 Interrupt .............................................. 87
  C.1.5 Timer45 Interrupt ............................................. 87
  C.1.6 Handshaking Initialization ................................. 87
  C.1.7 Handshaking Function ....................................... 87

C.2 Slave Microcontroller Functions ................................. 87
  C.2.1 Main Function ................................................. 87
  C.2.2 Device Initialization ....................................... 87
  C.2.3 Handshaking Initialization ................................. 87
List of Figures

2.1 Modular multilevel converter (MMC) topology ........................................ 5
2.2 Schematic of a half-bridge sub-module and its switching states (green represents a conducting switch, red Xs represents a nonconducting switch) .... 6
2.3 Schematic for MMC analysis ................................................................. 8
2.4 Representative NLC output from lower arm of MMC .............................. 12
2.5 Single phase converter AC voltage output using NLC (the dashed lines shows the reference wave) ............................................................ 13
2.6 LSC-PWM modulated output waveform using 5 contiguous carriers (the dashed lines shows the reference wave) ................................. 14
3.1 MMC simulation schematic ................................................................. 21
3.2 Simulation of an LSC-PWM based control system for an MMC ............ 22
3.3 Comparison of outputs for 5-level LSC-PWM (left) and 7-level NLC (right) 24
3.4 Simulation results for upper capacitor voltages using LSC-PWM ............ 25
3.5 Simulation results for upper and lower arm currents using LSC-PWM .... 26
4.1 MMC sub-systems ............................................................................. 29
4.2 Schematic of gate driver circuitry ....................................................... 33
4.3 Visualization of the quick sort operation [1] ....................................... 43
4.4 Capacitor voltage measurement system ............................................. 48
4.5 Arm current direction measurement system ........................................ 53
4.6 Firing pulses generated for upper and lower arms during start-up ......... 59
<table>
<thead>
<tr>
<th>Figure</th>
<th>Description</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>4.7</td>
<td>Capacitor discharge system</td>
<td>60</td>
</tr>
<tr>
<td>5.1</td>
<td>Output waveform of the three sub-module prototype</td>
<td>66</td>
</tr>
<tr>
<td>5.2</td>
<td>LSC-PWM outputs from microcontroller</td>
<td>67</td>
</tr>
<tr>
<td>5.3</td>
<td>Current Direction Measurement System</td>
<td>68</td>
</tr>
<tr>
<td>5.4</td>
<td>Sub-modules</td>
<td>69</td>
</tr>
<tr>
<td>5.5</td>
<td>Converter arm test with three sub-modules and modulation index of 1</td>
<td>70</td>
</tr>
<tr>
<td>5.6</td>
<td>Converter arm test with three sub-modules and modulation index of 0.75</td>
<td>70</td>
</tr>
<tr>
<td>6.1</td>
<td>Revised gate driver design</td>
<td>73</td>
</tr>
<tr>
<td>A.1</td>
<td>Sub-module PCB layout</td>
<td>81</td>
</tr>
<tr>
<td>A.2</td>
<td>Data distribution PCB layout</td>
<td>82</td>
</tr>
<tr>
<td>A.3</td>
<td>DC link PCB layout</td>
<td>83</td>
</tr>
<tr>
<td>A.4</td>
<td>Current measurement PCB layout</td>
<td>84</td>
</tr>
<tr>
<td>C.1</td>
<td>This function is the main function of the master converter</td>
<td>88</td>
</tr>
<tr>
<td>C.2</td>
<td>This function calls the initialization functions of the LCD, keypad, interrupts, and port pins to interface with the second controller.</td>
<td>89</td>
</tr>
<tr>
<td>C.3</td>
<td>This function initializes the interrupt functions used by the reference controller.</td>
<td>90</td>
</tr>
<tr>
<td>C.4</td>
<td>This function determines the number of SMs to be inserted in the lower arm every time the Timer2 interrupts the main function.</td>
<td>91</td>
</tr>
<tr>
<td>C.5</td>
<td>This function changes the display of the LCD every two seconds by interrupting the main function.</td>
<td>92</td>
</tr>
<tr>
<td>C.6</td>
<td>This function initializes the port pins connected to the second microcontroller.</td>
<td>93</td>
</tr>
<tr>
<td>C.7</td>
<td>This function initiates the communication with the second controller every time Timer2 interrupts.</td>
<td>94</td>
</tr>
<tr>
<td>C.8</td>
<td>This function determines the firing pulses every time the primary controller sends data to this controller.</td>
<td>95</td>
</tr>
</tbody>
</table>
C.9 This function initiates the port pins connected to the MUX and ADC, as well as the pins that send the firing pulses.

C.10 This function initializes the port pins connected to the primary microcontroller.
List of Tables

1.1 Project Specifications and Requirements ...................................... 3
3.1 Component Selection ...................................................................... 18
3.2 Selected Sub-Module Capacitor and Arm Inductor .......................... 19
3.3 Simulation Parameters .................................................................... 23
4.1 Input Arguments to C Function for the Generation of 5 Contiguous Carriers 36
4.2 Resistive Dividers For Various Capacitor Voltages ......................... 49
5.1 Voltage Measurement Data for Valve Test ...................................... 69
B.1 Project budget ............................................................................... 86
## Nomenclature

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>AC</td>
<td>Alternating Current</td>
</tr>
<tr>
<td>ADC</td>
<td>Analog-Digital Converter</td>
</tr>
<tr>
<td>DC</td>
<td>Direct Current</td>
</tr>
<tr>
<td>HVDC</td>
<td>High Voltage Direct Current</td>
</tr>
<tr>
<td>IC</td>
<td>Integrated Circuit</td>
</tr>
<tr>
<td>KCL</td>
<td>Kirchoff’s Current Law</td>
</tr>
<tr>
<td>KVL</td>
<td>Kirchoff’s Voltage Law</td>
</tr>
<tr>
<td>LED</td>
<td>Light-Emitting Diode</td>
</tr>
<tr>
<td>LCD</td>
<td>Liquid Crystal Display</td>
</tr>
<tr>
<td>MOSFET</td>
<td>Metal-Oxide Semiconductor Field-Effective Transistors</td>
</tr>
<tr>
<td>MMC</td>
<td>Modular Multilevel Converter</td>
</tr>
<tr>
<td>MUX</td>
<td>Multiplexer</td>
</tr>
<tr>
<td>NLC</td>
<td>Nearest Level Control</td>
</tr>
<tr>
<td>PSCAD</td>
<td>Power Systems Computer Aided Design</td>
</tr>
<tr>
<td>PWM</td>
<td>Pulse-Width Modulation</td>
</tr>
<tr>
<td>RMS</td>
<td>Root Mean Squared</td>
</tr>
<tr>
<td>SM</td>
<td>Sub-Module</td>
</tr>
<tr>
<td>THD</td>
<td>Total Harmonic Distortion</td>
</tr>
<tr>
<td>VFD</td>
<td>Variable-Frequency Drive</td>
</tr>
<tr>
<td>VSC</td>
<td>Voltage-Source Converter</td>
</tr>
</tbody>
</table>
Chapter 1

Introduction

The purpose of this project was to design a variable-frequency drive (VFD) using a multilevel circuit topology. The following sections of this chapter include project motivation, objectives, and specifications.

1.1 Motivation

Power electronic converters are widely used in many areas of electrical engineering and are becoming more prevalent in power systems in order to improve controllability and performance. In today’s high voltage direct current (HVDC) and motor drive industries a particular type of converter, namely the voltage-source converter (VSC) is heavily used. The common topologies of voltage source converters in operation today are two and three level pulse-width modulated VSCs (PWM-VSCs) [2]. Pulse-width modulation VSCs often require a series connection of semiconductor switches levels to meet voltage levels. High switching frequencies and/or filters are usually required to meet harmonic distortion requirements for PWM-VSCs[3].

The class of VSCs known as multilevel converters are gaining popularity as they offer better harmonic quality and reduce switching frequencies by producing multiple output
Modular Multilevel Converter

1.2 Project Objectives

This project demonstrates a proof-of-concept MMC prototype for use as a variable-frequency drive. The converter is used as an inverter which converts a DC voltage to an AC voltage. The converter utilizes a microcontroller-based control system that features a user adjustable frequency and voltage.

1.3 Project Specifications

Well-designed multilevel converters have been shown to be capable of producing low harmonic distortion at the output and as such that was the primary focus. The switching frequency and efficiency of the converter were not considered as critical design components in the final design as it was intended to be a prototype that can be improved upon in the future. The specifications for the MMC are summarized in table 1.1.
Table 1.1: Project Specifications and Requirements

<table>
<thead>
<tr>
<th>Converter requirements</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>DC-link voltage</td>
<td>250 V</td>
</tr>
<tr>
<td>Nominal power output</td>
<td>100 W</td>
</tr>
<tr>
<td>Nominal frequency range</td>
<td>50-60 Hz</td>
</tr>
<tr>
<td>Total distortion for harmonic orders $&lt; 15^{th}$</td>
<td>5%</td>
</tr>
<tr>
<td>Minimum number of output levels</td>
<td>4</td>
</tr>
</tbody>
</table>

The converter utilizes a 250V DC voltage source that is available in the Manitoba Hydro Power Systems Research Suite at the University of Manitoba and performance data is collected with Lab-Volt Electromechanical Systems available the laboratory. The converter is required to supply a resistive-inductive load consuming at least 100VA of apparent power at the full output voltage. The converter is specified to be able to output a voltage total harmonic distortion from orders 1 to 15 less than 5% in a frequency range of 50-60Hz. Table 1.1 summarizes the project specifications and requirements.
Chapter 2

Background

This chapter introduces the fundamental concepts of the MMC. A high-level circuit is presented in section 2.1 followed by the analysis of the elementary building blocks in section 2.2. The analysis of an ideal converter is shown in section 2.3 and the basic control is discussed in section 2.4.

2.1 Converter Topology

The MMC uses a repetitive structure with fully controlled, cascaded sub-modules. Figure 2.1 shows the circuit for a single-phase converter with $N$ sub-modules per arm. The series connection of the SMs in one half of the converter forms a valve, the inclusion of the arm inductor ($L_{arm}$) forms an arm, and the combination of the two arms forms a leg. The SMs are controlled in each valve to produce an alternating voltage $v_{ac}(t)$ between the mid-point of the two converter arms and the dc-link capacitors ($C_{DC}$).
2.2 Half-Bridge Sub-Modules

There are several types of sub-module topologies that can be used with an MMC [7]. This project was designed and built with half-bridge sub-modules as they require fewer components and utilize a simpler control scheme compared to more elaborate SMs. The SMs are either inserted to add voltage, or bypassed to allow current flow with no added
Ideally, T1 and T2 are complementary switches. A switch that is conducting is in the 'on' state and allows current flow in both directions. A switch that is nonconducting is in the 'off' state and current can only flow through the diode. A switch is considered on if it has sufficient gate-source voltage ($V_{GS}$).

Either the voltage potential from the capacitor ($U_C$) is inserted (on) in series in a valve with T1 on and T2 off, or no potential is added (bypassed) with T1 off and T2 on. It is
critical that T1 and T2 are never on simultaneously in order to avoid creating a short circuit across the capacitor which can result in damage and subsequent failure of the sub-module circuitry. Due to the finite and varying switching time of the switching devices and gate driver circuitry, a dead-time is required to ensure that one switch is completely off before the complementary switch conducts. The dead-time state occurs between the transitions of the SM from inserted to bypassed or vice-versa. The extended time of the SM producing $U_C$ or 0V at the output will result in a slight delay of output voltage. If both switches are off the potential output is dependent upon the instantaneous direction of current.

The capacitor voltage in a SM will increase or decrease depending upon the direction of current and switch configuration. The capacitor charging characteristics are shown for each switch configuration shown in figure 2.2. A SM inserted with $i(t)$ greater than zero will increase the capacitor voltage (charging), and a negative $i(t)$ will decrease the capacitor voltage (discharging). The capacitor voltage will not change if there is not current through it. If a SM is bypassed, the capacitor voltage remains constant assuming there is negligible stray current. During dead-time, the voltage of the SM capacitor will change only if the current is positive. The charging characteristics are important as they are used to balance the capacitor voltages associated with each SM as discussed in section 4.3.

### 2.3 Basic Converter Analysis

Consider the schematic shown in Figure 2.3
The total voltage in a valve is the sum of the voltages of each inserted sub-module in the respective valve and is labelled $v_U(t)$ and $v_L(t)$ for upper arm voltage and lower arm voltage respectively. The current through the upper arm travels through nodes 1-2-3 and is labelled $i_U(t)$. The current through the lower arm travels through nodes 3-4-1 and is labelled $i_L(t)$. The relationship derived from Kirchhoff’s Current Law (KCL) at node 3 is:
Applying Kirchoff’s Voltage Law (KVL) around the loop formed by nodes 1-2-3-1 yields

\[ v_{ac}(t) = -v_U(t) + \frac{V_{DC}}{2} - L_{arm} \frac{di_U(t)}{dt} \]  \hspace{1cm} (2.2)

Applying KVL around the loop 1-3-4-1 yields

\[ v_{ac}(t) = v_L(t) - \frac{V_{DC}}{2} + L_{arm} \frac{di_L(t)}{dt} \]  \hspace{1cm} (2.3)

Adding equations 2.2 and 2.3, dividing both sides by 2, and combining this result with equation 2.1 yields:

\[ v_{ac}(t) = \frac{v_L(t) - v_U(t)}{2} - L_{arm} \frac{di_{ac}(t)}{dt} \]  \hspace{1cm} (2.4)

Equation 2.4 demonstrates that the output ac voltage is proportional to the difference of the the voltages produced in each converter valve with an effective series impedance seen by half of the ac current. The need for an inductor in each converter arm is demonstrated by subtracting equations 2.2 and 2.3.

\[ L_{arm} \frac{d}{dt}[i_U(t) + i_L(t)] = V_{DC} - [v_U(t) + v_L(t)] \]  \hspace{1cm} (2.5)

Equation 2.5 shows that there exists a current flowing from the upper arm into the lower arm and not to the ac-side. This current is colloquially known as circulating current [8] and is damped by the arm inductance. The harmonic content of the circulating current stems from the difference between the dc-link voltage and the voltage produced in the converter leg. The circulating current can be reduced by controlling the converter such that the voltage produced in the leg is close to the dc-link $V_{DC}$ voltage shown in equation 2.6. During normal operation the total number of SMs inserted in the converter leg remains fixed.
in order to produce the dc-link voltage but the arm inductance, series resistance within the circuit, and changes in SM capacitor voltages prevent this.

\[ V_{DC} \approx v_U(t) + v_L(t) \]  

(2.6)

Assuming the voltage drop from the arm inductors is negligible, the upper and lower valve voltages can be respectively expressed as:

\[ v_U = \frac{V_{DC}}{2} - v_{ac} \]  

(2.7a)

\[ v_L = \frac{V_{DC}}{2} + v_{ac} \]  

(2.7b)

A modulation index \( m \) is set between 0 and 1 and is defined as the ratio of the maximum output voltage amplitude to one-half of the dc-link voltage. The output amplitude as a function of the modulation index control parameter is:

\[ V_{ac} = \frac{mV_{DC}}{2} \]  

(2.8)

Then the voltage that must be established in the upper and lower valves in order to produce a sinusoidal output with frequency \( f \) is:

\[ v_U(t) = \frac{V_{DC}}{2}(1 - m \sin 2\pi ft) \]  

(2.9a)

\[ v_L(t) = \frac{V_{DC}}{2}(1 + m \sin 2\pi ft) \]  

(2.9b)

Combining equations 2.9a, 2.9b, 2.4 and neglecting the effects of the arm inductance produces:
\[ \frac{V_{ac}(t)}{V_{DC}} = \frac{mV_{DC}}{2} \sin 2\pi ft \]  \hspace{1cm} (2.10)

Equation 2.10 shows the output voltage produced if each converter arm can produce
the ideal waveforms shown in 2.9a and 2.9b. The following section describes how the upper
and lower arms are controlled to obtain an output waveform closely representing equation
2.10.

2.4 Converter Control

If there are \( N \) sub-modules per arm and \( N \) sub-module are inserted in the converter
leg at all times, each capacitor will have a nominal sub-module voltage of \( V_{DC}/N \). If the
capacitor voltage is approximately nominal during operation, then a waveform consisting
of \( N + 1 \) discrete levels including zero can be generated in the upper and lower valves.
This section discusses how the upper and lower valves are controlled to generate a nearly
sinusoidal output voltage.

2.4.1 Nearest Level Control

Nearest level control (NLC) is a technique that chooses a discrete voltage level that is
closest to the reference value and places it at the output. The number of sub-modules to be
inserted in the upper and lower valves as a function of time can be calculated by resolving
equations 2.9a and 2.9b into \( N \) discrete levels by dividing by \( V_{DC}/N \) and rounding them
into the nearest integer.

\[ n_U(t) = \text{ROUND}[N \times \frac{1 - m \sin 2\pi ft}{2}] \]  \hspace{1cm} (2.11a)
\[ n_L(t) = \text{ROUND}[N \times \frac{1 + m \sin \pi ft}{2}] \]  \hspace{1cm} (2.11b)
From these two equations a similar relationship can be derived relating to equation 2.6.

\[ N = n_U(t) + n_L(t) \] \hspace{1cm} (2.12)

The ac-output voltage level is similar to equation 2.4

\[ n_{ac}(t) = \frac{n_L(t) - n_U(t)}{2} \] \hspace{1cm} (2.13)

Figure 2.4 shows the voltage waveform generated by the lower arm of a 5 SM MMC using NLC. The voltage in the upper arm of the converter is \( \pi \) radians out-of-phase from the voltage generated in the lower arm. Figure 2.5 is the output of the MMC obtained from equation 2.4. As can be seen, the MMC output is in phase with the voltage in the lower arm. The staircase waveform in figure 2.5 is the NLC representation of the sinusoidal reference waveform of equation 2.10. The accuracy of the representation largely depends on the number of SMs used and reaches an ideal sinusoid as \( N \) approaches infinity.

Fig. 2.4: Representative NLC output from lower arm of MMC
2.4.2 Pulse-Width Modulation

Pulse-width modulation (PWM) refers to the manipulation of the duration of a signal to produce certain desired characteristics. A sinusoidal reference is compared to a triangular or sawtooth carrier wave of a much higher frequency and the same amplitude to effectively shift harmonic content in order to filter it easier. The nature of a PWM signal is defined by two main properties which are its duty cycle and frequency. The duty cycle of the signal represents the fraction of time a controlled switch will be on in one period or cycle. The frequency determines the duration of a cycle.

2.4.3 Level-Shifted Carrier Pulse Width Modulation

Level-shifted carrier pulse width modulation (LSC-PWM) is used in converters with multilevel topology because the technique supports multiple carrier arrangements and mod-
ularity. The method is based on an amplitude difference or shift between carriers where each carrier is linked with a voltage level. Suppose \( N \) voltages have to be synthesized. \( N \) independent carriers are generated with the same frequency and amplitude. When the lower frequency converter arm reference voltage exceeds a carrier, the voltage level corresponding to that carrier is generated. This is done continuously under normal operation. The resulting waveform is a symmetric pulse train modelling a sinusoidal wave given the converter a switching frequency of \( f_c/N \) where \( f_c \) is the frequency of the carrier [2]. Several simulations were performed in order to determine the feasibility of this technique and one case is demonstrated in section 3.2.3. The LSC-PWM technique was shown to produce better harmonic performance compared to PWM and NLC.

Figure 2.6 shows five level-shifted triangle carrier waveforms, the sinusoidal reference waveform, and the modulated ac output waveform. The implementation of this technique is discussed in detail in section 4.2.

![Inserted Sub-Modules for Lower Arm using 5-Level LSC-PWM](image.png)

**Fig. 2.6:** LSC-PWM modulated output waveform using 5 contiguous carriers (the dashed lines shows the reference wave)
Chapter 3

Preliminary Converter Design

This chapter discusses the methodology used to design the converter’s main passive components and it’s control system. Section 3.1 details the methodologies used to determine the sub-module capacitor and arm component values, and section 3.2 gives an overview of the MMC simulation.

3.1 Sub-Module Capacitor and Arm Inductor Selection

The essential passive components in the MMC are the sub-module capacitors and arm inductors. The sub-module capacitors store charge and are inserted or removed in series to produce a desired output voltage. The arm inductors are required to reduce current flowing through the converter leg due to imbalances between the dc-link and the converter leg. The dc-link capacitors were provided by the ECE department and have a capacitance of 1000μF and voltage rating of 500V.
### 3.1.1 Sub-Module Capacitor

The sub-module capacitance is selected to limit the voltage ripple to an acceptable value under loaded operation. The rate of change in a capacitor’s voltage is inversely proportional to its capacitance for a given current through a capacitor from \( \frac{dV_{CC}}{dt} = \frac{i_c(t)}{C} \). A larger sub-module capacitor value increases the amount of stored energy in the converter and will result in less voltage deviation from a given nominal value. A suggested expression for a sub-module capacitor value for a three-phase converter is provided in reference [9] and is shown in equation 3.1

\[
EP = \frac{E_{nom}}{S} = 6N \times CV^2 \quad (3.1)
\]

In 3.1 EP is a proportional constant that represents the ratio of the nominal energy stored in the converter \( E_{nom} \) to the rated output apparent power, \( N \) is the amount of sub-modules per arm, \( C \) is the capacitor value of each sub-module, \( V \) is the nominal voltage across each capacitor, and \( S \) is the rated apparent power of the converter. EP is suggested to be in the range of 10-50mJ/VA to maintain approximately a 10% ripple in capacitor voltage for an operating frequency of 50Hz[9]. The \( 6N \) term in equation 3.1 was replaced with \( 2N \) to satisfy our requirements using a single-phase converter, and is rearranged to produce equation 3.2.

\[
C = EP \times \frac{NS}{V^2_{DC}} \quad (3.2)
\]

### 3.1.2 Arm Inductor

The arm inductor is chosen to limit circulating current and the rate of change of the current. Using too high of an arm inductance introduces a large output impedance
which consumes excessive reactive power and reduces transient speed of the converter. Reference [10] analytically shows that the second harmonic is the dominant harmonic of the circulating current and contains higher even orders. If \( N \) sub-modules are on at all times between the upper and lower arms, the effective series capacitance through the converter leg is \( C/N \). The effective series inductance is \( 2L_{\text{arm}} \) since there is an inductor for each arm. Another consideration for selecting the arm inductor is to avoid resonance with the effective capacitance. Resonance between the effective capacitance and arm inductance could result in an exceedingly high current through the converter leg in practical applications. The angular resonant frequency is given in equation 3.3.

\[
\omega_r^2 = \frac{1}{2L_{\text{arm}}} \frac{N}{C}
\] (3.3)

The arm inductance was chosen to resonate at a frequency lower than twice the fundamental since the circulating current is composed of second and higher order harmonics. Rearranging equation and applying a safety factor of 5/3 yields

\[
L_{\text{arm}} \geq \frac{5}{3} \times \frac{N}{2(2 \times 2\pi f)^2 C}
\] (3.4)

### 3.1.3 Capacitor and Inductor Finalization

The selection of the main passive components was based on component availability, price, voltage and current ratings, and their satisfaction of equations 3.2 and 3.3. The voltage ratings are proportional to the dc-link voltage and inversely proportional the number of sub-modules, while the current ratings will increase with the output apparent power \( S \).

The converter was initially intended to supply 175W with a 340V DC-link to produce a 120V RMS output. Assuming 4 sub-modules per arm were used, each capacitor would have to have a minimum rating of 85V. Assuming an output apparent power of 200VA at full output voltage, the peak output current is the twice the output power divided by the
peak output voltage. Assuming each arm contributes to one-half of the output current and including a 60% safety factor to include circulating current, then adding a DC-component from the dc-link, the peak current in each arm will be:

\[ I_{\text{max}} = 1.6 \times \frac{1}{2} \frac{2S}{V_{\text{DC}}/2} + \frac{P}{V_{\text{DC}}} = 2.4 \text{A} \quad (3.5) \]

A preliminary calculation using equation 3.2 with a corresponding capacitor is shown in table 3.1. The energy-power ratio and the number of sub-modules in the converter arm were chosen to maximize the required capacitance in order to minimize the amount of required sub-modules. The operating frequency was reduced to the minimum value the converter specifies in order to maximize the required arm inductance. The apparent power and dc-link voltage were chosen to reflect an older version of our project specifications.

<table>
<thead>
<tr>
<th>( f ) [Hz]</th>
<th>( N )</th>
<th>( EP ) [J/VA]</th>
<th>( S ) [VA]</th>
<th>( V_{DC} ) [V]</th>
<th>( C ) [( \mu \text{F} )]</th>
<th>( L_{\text{arm}} ) [mH]</th>
</tr>
</thead>
<tbody>
<tr>
<td>50</td>
<td>6</td>
<td>0.05</td>
<td>200</td>
<td>340</td>
<td>520</td>
<td>24</td>
</tr>
</tbody>
</table>

Finding an affordable inductor in the tens of millihenry range was difficult due to the required current rating for the design. Since the arm inductor in equation 3.4 is inversely proportional to the sub-module capacitance, the sub-module capacitor value would ultimately be increased to reduce the arm inductance required. An increase in sub-module capacitance allows for smaller inductor values with a lower voltage ripple, but comes at the expense of greater energy stored in the converter. The larger amount of energy stored in the converter necessitated the design of a capacitor discharge system discussed in section 4.8.

Affordable capacitors in the millifarad range rated to 100V were available for individual sale and corresponding arm inductances were calculated using equation 3.4 until an accept-
able combination was found. The component values including worst case scenario tolerances were tested in an MMC simulation case to ensure adequate performance. A summary of the final component selection is shown in table 3.2.

<table>
<thead>
<tr>
<th>Sub-Module Capacitance</th>
<th>Arm Inductance</th>
</tr>
</thead>
<tbody>
<tr>
<td>Value</td>
<td>2.2 ± 10% mH</td>
</tr>
<tr>
<td>Voltage Rating</td>
<td>N/A</td>
</tr>
<tr>
<td>Current Rating</td>
<td>4A</td>
</tr>
<tr>
<td>Part Number</td>
<td>ESMH101VSN682MA50T</td>
</tr>
<tr>
<td>Type</td>
<td>Aluminum</td>
</tr>
</tbody>
</table>

The selected capacitance was $6800 \mu F$ [11] which results in an arm inductance 1.86mH using 6 sub-modules per arm and 50Hz with equation 3.4. 2.2mH inductors [12] were purchased as they were greater than the recommended value to avoid resonance. The corresponding resonant frequency for a circuit with an inductance of $2L_{\text{arm}} = 2 \times 2.2 \text{mH}$ and capacitance of $C/N = 6800 \mu F/6$ is 71Hz and below twice the minimum fundamental frequency which is 100Hz.

3.1.4 Future Design Flexibility

The choice of sub-module capacitance for this design can also be applicable if the converter power rating or the number of sub-modules is to increase for a future improvement. The selection of the sub-module capacitor turned out to be much larger than the one suggested by equation 3.2 and would perform adequately for higher rated output power. Since there are many more capacitors in the MMC than there are arm inductors, it was determined to be a more economical decision to over design the capacitors initially as
there would be less components to replace. Lower operating frequencies would also require
an increase in arm inductance as the resonant frequency of the circulating current would
decrease.

3.2 Simulation

A high-level simulation model was developed and utilized throughout this project as a
means to test the converter design concepts and verify design decisions. The detailed model
was developed on Power Systems Computer Aided Design (PSCAD) using the component
values chosen in section 3.1.3 to reflect the final hardware design. The simulation results
were used to select the control technique discussed in section 4.2. The finalization of com-
ponent values and control techniques were completed by analyzing the results of simulation
cases with various parameters and is discussed in section 3.2.3.

3.2.1 MMC Modelling

A simulation timestep of 5µs was considered sufficiently small in order to accurately
analyze the parameters of interest. The detailed model uses an ideal control system with no
computational delay or dead-time. Series resistances in the range 0.1 - 10 ohms and switch
voltage drops of 0.7V modelled non-idealities in the circuit. The schematic for a 5-level
simulation case is shown in figure 3.1. The series resistances are outlined with a red box,
and the current and voltage measurement system models are outlined in green in figure 3.1.
The simulation model allows for adjustments in output frequency and voltage during the simulation in order to permit the transient analysis of the converter. The frequency and modulation index control parameters are passed to the MMC block where the control...
Figure 3.2 shows the schematic of the control system for an LSC-PWM control system.

The reference and carrier waveforms are generated based on a modulation index, frequency, and number of active sub-modules as discussed in section 2.4.3. The number of inserted sub-modules in the upper and lower arms is determined in the LSC Modulation block by evaluating the number of carriers that are less than the reference waveform at any given instant in time. The Sort and Fire blocks determines which sub-modules should be inserted based on the direction of current, and the change state of the individual capacitors. FORTRAN was used to program the LSC Modulation and the Sort and Fire blocks.
3.2.2 Simulation Parameters

Table 3.3 shows the ranges of simulation parameters that were tested.

<table>
<thead>
<tr>
<th>Fixed Parameters</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>DC-Link Voltage</td>
<td>250V</td>
</tr>
<tr>
<td>DC-Link Capacitance</td>
<td>1000µF</td>
</tr>
<tr>
<td>Sub-Module Capacitance</td>
<td>6800µF</td>
</tr>
<tr>
<td>Arm Inductance</td>
<td>2.2mH</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Varying Parameters</th>
<th>Range</th>
</tr>
</thead>
<tbody>
<tr>
<td>N (SM/arm)</td>
<td>4 to 6</td>
</tr>
<tr>
<td>Frequency</td>
<td>50 and 60Hz</td>
</tr>
<tr>
<td>Modulation Index</td>
<td>0.5 - 1</td>
</tr>
<tr>
<td>Load Resistance</td>
<td>25-300Ω</td>
</tr>
<tr>
<td>Load Inductance</td>
<td>0.05-1.6H</td>
</tr>
<tr>
<td>Control Techniques</td>
<td>Nearest Level Control (NLC)</td>
</tr>
<tr>
<td></td>
<td>LSC-PWM with $f_c = 27 \times f$</td>
</tr>
</tbody>
</table>

The output power and harmonic distortion were calculated on PSCAD for several different combinations of the parameters shown in table 3.3. Two examples of the simulation results using different control schemes are demonstrated in the following section.

3.2.3 Simulation Results

The final selection of the main components and control scheme were verified through the simulation results presented in this section. Nearest level control was used with 6 sub-modules per arm, and LSC-PWM was used with 4 sub-modules per arm with a carrier frequency 27 times the fundamental frequency of the reference. Both converter configura-
Simulations generated a 50Hz output waveform with a modulation index of 1 to provide 88.4V RMS. The actual output voltage of the converter was expected to be lower due to voltage drops across the switches, series resistance, and the arm inductors in the converter. A resistive-inductive load of 57.1Ω and 0.07619H was chosen as it could readily be made with Lab-Volt equipment and tested with the physical converter that was built. A comparison of the output voltages and currents are shown in figure 3.3

Fig. 3.3: Comparison of outputs for 5-level LSC-PWM (left) and 7-level NLC (right)
Both simulation cases resulted in an output voltage waveform with a fundamental component equal to 84V RMS and a power output of approximately 98W. The harmonic distortion for orders 2-15 of the LSC-PWM simulation totalled 4.9%, while NLC resulted in 8.4%. The harmonic performance using LSC-PWM with fewer sub-modules compared to NLC justified the use of LSC-PWM for our final design. Using the more advanced LSC-PWM allowed us to reduce costs and components by reducing the amount of required sub-modules. The sub-module capacitor voltage and arm current waveforms for the LSC-PWM simulation case are shown in figures 3.4 and 3.5 respectively.

Fig. 3.4: Simulation results for upper capacitor voltages using LSC-PWM
Figure 3.4 shows that the chosen sub-module capacitance value results in a capacitor voltage between 60.6V and 61V. The current waveforms predict that the current through the upper and lower arms will be a maximum of 1.5A. The voltage ripple is calculated as

$$\Delta U_C = \frac{U_{C,max} - U_{C,min}}{2} = \frac{61.0 - 60.6}{2} = 0.2V$$  \hspace{1cm} (3.6)$$

The simulation results predicted that 4-6 sub-modules per arm with a sub-module capacitance of 6800µF and arm inductance of 2200µH using LSC-PWM while supplying 98W at a power factor of 0.922 lagging to a fixed resistive-inductive load will meet the
project specifications. The selected sub-module capacitance resulted in a voltage ripple that was a small fraction of the nominal voltage. The selected arm inductance suppressed the circulating current levels such that they did not exceed the component ratings.
Chapter 4

MMC Sub-Systems

This project was divided into several sub-systems that were assigned to each group member or worked on as a team. The sub-systems were treated as independent tasks that were later integrated as discussed in chapter 5. Figure 4.1 provides an overview of each of the sub-systems and how they interact.

The switch and gate driver circuitry as well as the reference modulation control were considered the primary sub-systems for the hardware and control system respectively. Section 4.1 details the switch and gate driver sub-system while section 4.2 details the reference and modulation control. The capacitor sorting and balancing and the voltage and current measurement were considered secondary sub-systems as they serve as means of translating converter operating parameters between the primary sub-systems. The secondary sub-systems are discussed in sections 4.3 through 4.5. The user interface, starting routine, and capacitor discharge systems were considered auxiliary features of the converter. Section 4.6 through 4.8 detail the auxiliary components. Finally, printed circuit boards (PCBs) were used to mount the converter hardware for this project. The design and fabrication of the PCBs is discussed in section 4.9.
4.1 Switch and Gate Driver Circuitry

The gate driver circuit serves as the interface between the low voltage control system and the high voltages required for waveform generation by the switches in a sub-module. This section discusses the selection of the switches in 4.1.1 and the associated components in 4.1.2 to 4.1.4. The components involved in the gate driver circuit are the gate driver integrated circuit (IC), optocouplers and dead-time generators. The gate driver is discussed in section 4.1.5 and an alternative circuit is proposed in 6.2.
4.1.1 Switches

The selection of switches for every sub-module is a key part of the design process. Power MOSFETS were chosen over IGBTs for this project because of their lower power rating requirements [13]. The switches used for each SM are the International Rectifier IRFI4019HG-117P [14]. The IRFI4019HG-117P combines two switches in one package; each switch having its own anti-parallel diode. This feature reduces the amount of components and lowers the amount of fabrication required for each SM. The voltage rating of each switch and diode is 150V which is above the designed nominal voltage of each sub-module capacitor. The maximum continuous current rating of each of the switches within the IRFI4019HG-117P is 8.7A and well above the simulated operating current.

During switching operations of a power MOSFET, there can be a large changes of current with respect to time. This rate of change of current can cause large voltage spikes due to stray inductance within the gate driver circuit and switches. A small series resistance placed between the gate of the power MOSFET and the gate driver IC reduces the switching speed of the power MOSFET. A slower switching speed decreases the \( \frac{di}{dt} \) and therefore limits the voltage spikes. A value of 10Ω was chosen so as to reduce the voltage spikes while keeping the turn off time as low as possible in accordance to the switch’s data sheet. Further protection considerations for the sub-module switches are discussed in chapter 6.1.

4.1.2 Gate Driver Integrated Circuit

A MOSFET driver IC is used to translate a low voltage input from the microcontroller to a suitable level to operate the power MOSFET. The gate driver IC must be able to source and sink charge to the power MOSFET gate terminal in order to turn the switch on. Due to the topology of the MMC, both switches in all but one sub-module will have a reference potential greater than earth ground and floating. One of the requirements of the gate driver
IC is to be able to work correctly under these conditions. For this reason, the International Rectifier IR2118 [15] was chosen. The IR2118 is designed to supply switches whose reference potential (source) is an elevated voltage with respect to the control ground up to 600V and well above our operating voltage.

4.1.3 Optocoupler

Electrical isolation between the gate driver circuit and the microprocessor is provided by using optocouplers. Optocouplers transmit the electrical signal across an electrical barrier by using light emitting diodes. The optocoupler chosen are the Fairchild H11L1M [16] where the outputs use schmitt triggers to provide noise immunity. The H11L1M was selected for it’s high data transfer rate at 1MHz relative to our converter’s switching frequency. The output voltage of the H11L1M is also sufficient to meet the gate driver IC’s input threshold.

4.1.4 Dead-Time Generator

The dead-time generator ensures both sub-module switches are never on simultaneously. The dead-time generator chosen is the IXYS IXDP630 [17]. The IXDP630 converts a single firing command from the microcontroller into two complementary outputs to the upper and lower switches of the sub-module. Each IXDP630 is capable of operating up to three sub-modules independently with the same time delay. The firing signal from the dead-time generators is passed to the optocouplers. The dead-time accounts for the on and off time of the optocoupler, gate driver IC, and switching time of the power MOSFET switches while also keeping the latency between the microcontroller and the power MOSFETs to an acceptable level. The dead time of the IXDP630 is fixed at 8 clock cycles where the clock frequency of the device is controlled by an external RC network given by the following equation:
A dead-time of approximately $1.6\,\mu s$ was chosen and experimentally verified using a clock resistance of $3.3\,k\Omega$ and a capacitance of $47\,pF$. The on and off time difference between the optocouplers [16] is typically $0.2\,\mu s$ and the on and off time for the gate driver IC [15] is $0.05\,\mu s$. The switches have an on and off time difference in the order of nanoseconds. A dead-time of $1.6\,\mu s$ exceeds the sum of the on and off time delays by over $1\,\mu s$ ensuring sufficient dead-time. The dead-time can be easily changed if the performance of the converter is hindered too much. Another feature of the dead-time generator is it’s ability to disable all of it’s outputs. This feature allowed for the connection of a physical switch to bypass the microcontroller and open all of the sub-module switches in the converter to a dead-time state if needed.

### 4.1.5 Gate Driver Implementation

Figure 4.2 shows a schematic of the gate driver components. The dead-time generators are not shown as they were placed on a different PCB as discussed in 4.9. The optocouplers receive their inputs from the dead-time generator with respect to the control system ground. The optocouplers chosen are active low devices and as such the gate drivers were chosen to have an inverted input. The optocoupler’s output and gate driving input are supplied with a $12V$ supply with respect to converter ground which can be isolated from the control system ground. For this project, the control system ground and converter ground are tied at one point in the system.
Fig. 4.2: Schematic of gate driver circuitry
The gate driver capacitors (10µF and 1µF) are supplied through a DC/DC converter (shown in figure 4.2 as [5-15] in the green label). One electrolytic and one ceramic capacitor is connected in parallel to provide charge to the upper and lower MOSFET gates. The electrolytic capacitors provide low equivalent series resistance for decoupling, while the ceramic capacitor provides better frequency response at higher frequencies.

The reference of each sub-module (labelled SM- in the red box in figure 4.2) changes as sub-modules connected below it are inserted or bypassed. This can result in a fast-changing high common mode of each sub-module capacitor with respect to converter ground. The changing reference is shown as an alternating source labelled 'Positive Swinging Voltage'. The output reference of the DC/DC is tied to the source of the lower MOSFET to ensure that the gate driving capacitors receive a voltage 15V with respect to the respective switch sources. This technique is referred to as bootstrapping. A gate-to-source voltage of 15V was chosen to ensure the MOSFET functions correctly in its operating region and reduces the drain-source resistance during operation. The chosen MOSFET datasheet [14] suggests that in order to guarantee the operation of the power MOSFET for higher currents, the gate to source voltage must be above 10 V. As T1 and T2 are complementary switches, when T1 is on and T2 is off, the lower gate driving capacitor receives charge from the DC/DC converter. When T1 is off and T2 is on, the upper gate driving capacitor is charged through the bootstrapping 1N4148 diode.

During the initial design period, 5/15V DC/DC converters were purchased as the control system supply voltage was assumed to be 5V. Microcontroller project boards were donated for this converter that run on 3.3V supply, and as such either an alternative voltage supply had to be used, or new DC/DC converters had to be purchased. To reduce the amount of supply voltages to the sub-module, a 5V regulator was added so that only a 12V supply would be required for the gate-driver circuitry and the purchase of more DC/DC converters could be avoided. Section 6.2 shows a revised gate driver circuit that reduces the number
sub-module power supplies.

4.2 Reference and Modulation Control

4.2.1 Implementation

A sinusoidal reference waveform was generated using a microcontroller. The value of this waveform at different sampling points will determine the number of SMs inserted or bypassed in each arm of the converter. The goal is to modulate the reference to produce an output voltage consisting of a quantized digital signal that is representative of the reference waveform. The reference will be modulated in such a way that the fundamental frequency at the output of the MMC will be the same as the fundamental frequency of the reference. This means that the frequency at the output of the MMC can easily be changed by changing the frequency of the reference waveform.

A factor called the modulation index is used to scale the peak to peak amplitude of the reference. By changing the modulation index of the reference, we can obtain different properties at the output of the waveform. The modulation index is between 0 and 1 in its linear range and is usually expressed as a percentage. A modulation index greater than 1 will lead to over-modulation and will result in a reconstruction of the reference signal. In some applications, it may be acceptable to operate within 10-20% of the linear range. This is usually done when certain harmonic components are desired.

In section 2.4.3, the basics of LSC-PWM was introduced. 5 contiguous carrier waveforms were generated and used to modulate the reference. The carrier of choice was a continuous triangle wave that were modelled by taking samples of two lines with slopes of equal magnitude, but with opposite signs, and the same peak to peak amplitude. The carriers were generated by creating a microcontroller based C function that models straight lines, with slope $m$ and $y$-intercept $b$ as given by equation 4.2 below:
\[ y = \pm mx + b \] (4.2)

The input arguments to the function are the slope of the line and the y-intercept of the line. The function returns an array of discrete values. Both lines generated are then combined to form a complete triangle inside the function. A plot of the values generated by the function accurately models a single triangle waveform carrier. The input arguments to generate all 5 carriers needed for LSC-PWM are given in table 4.1.

<table>
<thead>
<tr>
<th>Carrier</th>
<th>Slope, ( m )</th>
<th>y-intercept, ( b )</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>2</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>3</td>
<td>1</td>
<td>2</td>
</tr>
<tr>
<td>4</td>
<td>1</td>
<td>3</td>
</tr>
<tr>
<td>5</td>
<td>1</td>
<td>4</td>
</tr>
</tbody>
</table>

It is important that the carrier waveforms are all generated in phase and never lose synchronism during normal operation. Out-of-phase waveforms will lead to an abysmal voltage waveform at the output of the MMC.

It is easy to note from table 4.1 and figure 2.6 that the carriers all have an amplitude of 1 p.u peak to peak. This is because the sinusoidal wave reference generated for the technique is required to have an amplitude that is an integer multiple of the number of SMs in order to operate fully within the linear modulating range. Hence, the contiguous carriers have to span the entire reference amplitude vertically. The amplitude of the reference will be chosen to be 5 p.u peak to peak for simplicity.

Thus far, we have mentioned the C function for generating a triangle carrier. However,
a single triangle does not necessarily create a repeated wave with measurable frequency. In PWM the carrier(s) are required to have a fundamental frequency component that is much greater than that of the reference waveform [18]. For this project, the maximum operating frequency is 60Hz and as a rule of thumb, the carrier should have its fundamental frequency to be at least 15 times that of the reference. This makes the minimum carrier frequency out to be 900Hz. However, the higher the frequency of the carrier, the more comparisons can be made between the carrier and the reference. A higher carrier frequency will also result in more switching losses because there will be significantly more switching instances within the converter. A compromise has to be made as the carrier frequency cannot be unwisely increased. To tackle this dilemma, we put a few things into consideration:

- Carrier frequency should be odd and a multiple of 3
- Prevention of audible acoustic noise while driving a load
- Switching and harmonic losses
- THD requirement of the converter

Choosing a carrier frequency that is a multiple of 3 will make for future provisions of improving the converter to 3-phase much more feasible. Likewise, as discussed previously, the carrier frequency can only be increased up to a certain point; that point can be said to be when the switching and harmonic losses are deemed unacceptable. Also, although acoustic noise is not as much relevant as the other two considered factors, it can play a role if the load driven is a variable speed induction motor.

After simulating various scenarios, it was found that to achieve the THD requirement that was established in the proposal, we will require a carrier frequency of at least 21 times the fundamental frequency of the reference. Also, after estimating the switching losses for each simulation done, a maximum carrier frequency was set at 30 times the fundamental
frequency of the reference waveform. The carrier frequency decided upon was arbitrarily chosen to be 27 times the fundamental frequency of the reference, therefore setting the carrier frequency at 1620Hz.

To this point, a carrier signal with measurable frequency is yet to be established as we have not established how we transpose one triangle into a continuous signal. By definition, a carrier frequency that is 27 times that of the frequency of the reference means that for every one cycle of the reference, there are 27 cycles of the carrier. Also, the C function that creates the triangle returns an array of discrete samples of a triangle wave. This means (in theory) that for one cycle of the reference, 27 replica arrays of the single carrier has to be created. There are 5 carriers in total to account for 5 SMs of the converter. This brings rise two fundamental problems:

- The microprocessor being used would have to be able to create enough memory space to accommodate 27x5 arrays of the carrier.
- This would be a very poor and inefficient design.

For this project, a continuous triangle wave was never achieved as a result of unrealistic microprocessor memory expectations. As mentioned in 2.4.3, the reference is sampled and compared to the 5 carriers and by that a voltage level is generated. This comparison is done every time the reference is sampled.

To explain the solution that was implemented, take for instance an array containing 48,000 samples of the reference sinusoid and an array containing 48,000 samples of one period of the carrier. Let’s assume a sample of the reference was taken at sample 28,493; to compare the elemental value of this sample with the carrier, the value of the carrier at this point in the wave has to be accurately determined. The knowledge of having 27 cycles of carriers for one cycle of reference leads to a simple solution as illustrated below:

- Total number of samples of reference in one cycle of reference: 48,000
- Total number of samples of carrier in one cycle of reference: 1,296,000

- Total number of samples of carrier available: 48,000

- Sampled sinusoid location: 28,493

- Sampled carrier location: $27 \times 28,493 = 769,311$

- Sampled carrier location (available): $[769,311 - 48,000n] < 48,000$ for $n = 0, 1, 2, 3$

- $769,311 - 48,000 \times 16 = 1,311$, $n = 16$

There are a few things to note that will clarify this solution:

- In the 1,296,000 carrier samples, there are only 48,000 unique samples

- The value of $n$ increases until the expression is between 0 and 48,000

What this solution provides is a way to avoid creating redundant arrays. It shows that sample 28,493 of 48,000 in the reference corresponds to sample 1,311 in an array of size 48,000 of the carrier. Since the carriers are contiguous and have the same peak to peak amplitude, this operation can be done only once to reduce computation time.

In order to determine the voltage level needed at the output, the sample of the reference waveform will be compared to the corresponding value of the lowest carrier level. If the reference value is larger than the carrier’s, the value of the reference will then be compared to the value of the carrier immediately above the previous one. This process will be repeated until the value of the sample taken from the reference is lower than a carrier; when this happens, the specific level of this carrier corresponds to the required voltage level needed at the output, and hence how many SMs needed to be inserted or bypassed. In the peculiar cases where the carrier is equal to the reference, then that voltage level is sent to the output; also, if the reference is larger than all of the carriers, then all of the SMs in the lower arm need to be inserted, and all of the SMs in the upper arm need to be bypassed.
The image in figure 2.6 below shows a clear representation of the theoretical expectations of the carrier arrangements and the sinusoidal waveform.

4.3 Capacitor Voltage Balancing and Sub-Module Sorting

Sub-modules contained in the same arm of the converter are connected in series, and will be subjected to the same amount of current. Therefore balancing within branches must be done through varying the output voltage of each SM while keeping the total output voltage of the branch ideally constant. The variation in the SM output voltage will only have significant effect on the capacitor voltage when the SM is enabled [19].

Balancing the capacitor voltages within each arm requires the capacitor voltages of a SM with a lower (than the required) voltage to be shifted up to have more charging time when the current is positive. If the current flowing through the arm is negative, the voltage is shifted down to have less charging time[20]. In the case where the voltage across the SM capacitor is higher (than required) the reverse operation is done to reduce the capacitor voltage. This process is done continually achieving the goal of constant net voltage across each arm.

In a real system like ours, this process is done using a microcontroller. The software is written in assembly language and in C. Once the voltages across each capacitor have been measured, they are scaled down to the range of 0-3.3V so that they can easily be read by the microcontroller. The voltages are then accepted by the microcontroller using an analog-digital converter and serially read by a multiplexer. The microcontroller also receives the direction of current from the current measurement system; it then passes this information to the balancing algorithm.
4.3.1 Balancing Algorithm

To balance the energy within the converter, the voltages across each capacitor first have to be sorted and stored in a reference list. There are several sorting algorithms that can be used. Since importance of efficiency and computation time is paramount, different algorithms were analyzed to determine which one was better suited for our purposes. Some of the factors that go into deciding what sorting algorithm to use may include one of the following:

- Size of the array to be sorted
- Programming language and data type to be sorted
- \( \text{Big-O} \) order of the algorithm
- Partially sorted, reversed, random, or half sorted array

Considering all of those factors, the algorithms of choice were narrowed down to the bubble sort and the quicksort.

4.3.2 Bubble Sort

If the position in an array is \( n \), then the bubble sort algorithm works by comparing the elements in array positions \( n \) and \( n+1 \) and performs a swap operation if the element in \( n \) differs from the element in \( n+1 \). In the forward pass method and ascending order sort, if the element in \( n \) is greater than the element in \( n+1 \), the element in \( n \) will be swapped with the element in \( n+1 \) and if the element in \( n \) was less than the element in \( n+1 \) then it will be passed. In the forward pass method and descending order sort, the reverse is the case. Put simply, depending on the direction of sort, the larger values will bubble up/down the array and the smaller values will bubble down/up the array.

The bubble sort provides very good performances in some cases and in other cases, it
can be very inefficient. Since the array to be sorted in this case was a relatively small array that we envisioned to have a maximum length of seven elements, the algorithm was worth investigating as it performs relatively well in small size arrays. The algorithm also does well in partially sorted arrays which was again what we expected to have since the voltages across the capacitors will not vary too much.

In its worst form, the bubble sort is of order $O(n^2)$ in the amount of comparisons to be made and $O(n^2)$ in amount of exchanges [21]. This will occur when the array is completely unsorted (random/selective scattered array). If the array happened to be sorted the algorithm improves to $O(n)$ comparisons and $O(1)$ exchanges [21]. Using average-case analysis of the algorithm, it was determined that using the bubble sort will increase the computation time in the balancing process.

### 4.3.3 Quick Sort

The quicksort algorithm works by selecting an element called the pivot\(^1\). The algorithm then performs a first pass through the array and places every element less than the pivot to the left of the pivot and every element greater than the pivot to the right of the pivot. On the second pass, a new pivot is selected (usually different than the first) and the operation is repeated. This process is done recursively until the array is completely sorted. This method is one of the fastest methods around because of its recursive nature. To explain this further, for simplicity, take for example an array containing 11 random elements; if the middle element is selected as the pivot, 5 elements less than that pivot will lie to the left and 5 elements greater than that pivot will lie to the right. Since this is done recursively, the 5 elements to the left will represent a new random array that will be sorted and also the 5 elements to the right. This will be a pattern that trickles down a tree in a method

\(^1\)The selection of a pivot can be systematic or random depending on the size of the array. For a small or medium size array, the first, middle or last element can be selected. The pivot for a larger array has to be chosen to achieve better efficiency.
similar to the binary search tree configuration as shown in figure 4.3 below.

![Visualization of the quick sort operation](image)

**Fig. 4.3:** Visualization of the quick sort operation [1]

In general, to more accurately analyze the effectiveness of the algorithm; let us assume that we have an array of size \( n \) and that selecting a pivot has divided the array into two parts (equal or unequal). Let us call the size of the first part \( k \), the size of the second part is invariably \( n - k \), and we can form the following relation:

\[
T(n) = T(k) + T(n - k) + \alpha n \tag{4.3}
\]

\( T(n) \) represents the time taken to sort the complete array of \( n \) elements and \( \alpha \) is an arbitrary constant determined by the partitioning arrangement and pivot selection.

If the selected pivot was to be the smallest element in the array, which will give us a worst case analysis, will divide the array into 1 and \( n - 1 \). Equation 4.3 becomes

\[
T(n) = T(1) + T(n - 1) + \alpha n \tag{4.4a}
\]

In the above relation, we can replace \( T(n - 1) \) by \( T(n - 2) + T(1) + \alpha(n - 1) \) by replacing
\( n = n - 1 \) in equation 4.3. The result yielded is

\[
T(n - 1) + T(1) + \alpha n = [T(n - 2) + T(1) + \alpha(n - 1)] + T(1) + \alpha n \quad (4.5a)
\]

\[
= T(n - 2) + 2T(1) + \alpha(n - 1 + n) \quad (4.5b)
\]

We can continue this operation and derive a pattern that can be expressed as:

\[
T(n) = T(k) + T(n - k) + \alpha n = T(n - i) + iT(1) + \alpha \sum_{k=0}^{i-1} (n - k) \quad (4.6a)
\]

To find the limit of \( i \), we can realize that \( i \) cannot grow larger than \( n - 1 \) because if that happens, \( n - i \) will be less than 1. Hence we can substitute the limit for \( i \) into the expression and obtain

\[
T(n) = nT(1) + \alpha(n(n - 2)(n - 2)(n - 1)/2 \quad (4.7)
\]

Notice the order of equation 4.7 is \( O(n^2) \).

If the pivot is chosen in such a way that it divides the array into two equal parts in every step we have the best case of quicksort (This can only be done systematically or very lucky successive guesses). Therefore both parts have sizes of \( n/2 \). We can do similar analysis as before but this time the recurrence will be of the form:

\[
T(n) = 2T\left(\frac{n}{2}\right) + \alpha n \quad (4.8)
\]

As before, if we keep substituting \( n - 1, n - 2, n - 3... \) for \( n \) in equation 4.8 we will obtain the form:
Modular Multilevel Converter 4.3 Capacitor Voltage Balancing and Sub-Module Sorting

\[ T(n) = 2^k T\left(\frac{n}{2^k}\right) + k\alpha n \]  

(4.9)

We can find the limit for \( k \) if we recognize that when \( 2^k > n \) the expression \( \frac{n}{2^k} < 1 \) hence the limit for \( k = \log n \). We can substitute that into equation 4.9 to yield:

\[ T(n) = nT(1) + n \log n \]  

(4.10)

The expression in equation 4.10 has the order of \( O(n \log n) \) as can be seen. It is easy to achieve the best case every time by finding the median of the array and using that element as the pivot. This can be done in several ways however the \textit{median – of – three} technique is more commonly used.

To avoid the worst case, the pivot can be chosen at random [22].

On average, the quick sort algorithm has the order of \( O(n \log n) \) [22]. However, proof of that goes beyond the scope of this report and is irrelevant to the project. This analysis however shows that on average, the quick sort algorithm is faster than the bubble sort and hence was the choice algorithm for the balancing scheme.

4.3.4 Methodology

The capacitor voltages upon being acquired are sent as analog data to the quicksort function in the microcontroller. The function performs the sort and returns an array containing the capacitor voltages in ascending order. However, this loses the address of the submodule corresponding to each capacitor voltage, hence a temporary array is created initially that replicates the original array before the sorting is done. The copy algorithm used is the deep copy; although this is a more expensive copy and slower copy algorithm, it is the only way to avoid memory addressing complications.

An array of \( k \) elements that will contain the firing pulses is created, with \( k \) being the size of the capacitor voltages array. The array elements are initialized to zero. The algorithm
then performs a check to confirm if the number of SMs to be inserted has changed or if the
direction of current has changed\(^2\). If this is the case, the sorted and unsorted arrays are
then compared. The index of each array ranges from 0 to \(k - 1\). Since the temporary array
contains the original unsorted voltage in their correct indexes, a linear search (Big-O \(O(n)\))
for each element in the temporary array is performed on the sorted array. If the current is
positive, and the number of SMs to be inserted is \(n\), then the algorithm selects the top \(n\)
voltages in the sorted array, and based on the indexes obtained from the linear search, the
correct firing pulses are determined. If however the current is negative, then the bottom \(n\)
voltages in the sorted array are selected. This process is done twice; once for the upper arm
of the converter and once for the lower arm of the converter. The only difference between
these two is if \(n\) SMs are to be inserted in the lower arm, then \(N - n\) SMs will be inserted
in the upper arm, where \(N\) is the total number of SMs in each arm.

4.3.5 Optimizing the Algorithm

Testing the algorithm using the microcontroller and ultimately the hardware, we re-
alized that we had limitations because the computation time was slow. The current mea-
surement was estimated to take about 200\(\mu\)s, the voltages were acquired in 270\(\mu\)s, while
the balancing algorithm also ran in 270\(\mu\)s which turns out to be 0.74ms. In one period,
if the number of SMs to be inserted changes 50 times (conservatively) then the total pro-
cessing time in one cycle will be 37ms which is too much time for our purposes. Hence,
some optimization had to be done while not sacrificing too much of the performance of the
converter.

Since the capacitors were overrated as discussed earlier, we could sacrifice balancing
the voltages every time the number of SMs to be inserted changed for a better systematic
balancing every \(\frac{1}{10}\) of the period. Hence, no matter how many samples are used to sample

\(^2\)sorting only occurs if one of the conditions is true for optimization purposes
the reference, the balancing algorithm will run only 10 times in one period reducing the computation time to 7.4ms from a conservative estimate of 37ms.

In a bid to achieve the best results, further optimization was done. Thus far, balancing is done \( \frac{1}{10} \) of a period. However, the voltage is not necessary acquired at the same time. Again, owing to the overrated capacitors, the voltages can be acquired 5 times in a period. Balancing is then done every time voltage is acquired hence reducing the number of balancing operations from 10 to 5. However, the algorithm still checks if the number of SMs to be inserted has changed every \( \frac{1}{10} \) of a period. If it has, it refers to the already sorted list and sends out firing pulses to the gate-drivers without a call to the quick sort function. This reduces the total computation time to about 4.8ms.

### 4.4 Sub-Module Capacitor Voltage Measurement System

As current flows through a loaded MMC, the voltage across each inserted capacitor changes. The comparison of voltages across each sub-module capacitor in an arm is required to balance the voltages by inserting sub-modules depending on the direction of current. Well balanced capacitor voltages reduces the capacitor’s voltage ripple, produces a more ideal output waveform, and reduces the circulating current through the converter legs. This section discusses the design of the capacitor voltage measurement system.

#### 4.4.1 Voltage Measurement System Design

The schematic for the capacitor voltage measurement system the MMC uses is shown in figure 4.4. The voltage measurement system uses a resistive divider to scale down the sub-module capacitor voltage, \( U_C \). The scaled down voltage is then fed to an isolating amplifier (ADuM3190 [23]) with unity gain that saturates at an input voltage of 2.7V. An isolating amplifier was chosen because all but one of the reference potentials of each sub-module (labelled SM- on figure 4.4) changes and is unpredictable as mentioned in 4.1.5.
The input side is powered through a DC/DC converter with its output reference tied to the reference potential of its submodule. The same DC/DC converter is used to supply the gate-driving capacitors discussed in section 4.1. The output side of the amplifier is powered through a 3.3V logic supply which is common throughout the control system.

**Fig. 4.4:** Capacitor voltage measurement system

Earlier test prototypes of the sub-modules used 9V batteries instead of the sub-module capacitor. The resistive divider shown by R1 and R2 in figure 4.4 was adjusted as the design progressed. Equations 4.11 and 4.12 were used to select the values for the resistive divider.

\[
V_{IN,\text{max}} = U_{C,\text{max}} \frac{R_2}{R_2 + R_1} \quad (4.11)
\]

\[
R_2 = \frac{R_1}{U_{C,\text{max}}/V_{IN,\text{max}} - 1} \quad (4.12)
\]

Assuming that the differential input impedance to the ADuM3190 is sufficiently higher
than the resultant R2, the input voltage to the ADuM3190 would be close to theoretical value shown in equation 4.11. Table 4.2 shows the calculated resistive dividers for various sub-module capacitor voltages. First, an R1 value was selected to reduce the current drawn by the divider. 9.1MΩ was selected as it is the highest available standard resistor. The maximum input voltage to the ADuM3190 was set to 2.4V to be less than the saturation voltage. R1 was calculated for various input voltages including a 9V battery and a 20V single MMC arm test that was conducted. The resistive divider for various numbers of sub-modules per arm (N) were also calculated with a 250V dc-link. The maximum capacitor voltage was treated as \( V_{DC/N} \) as the simulation results from 3.2.3 showed a small voltage ripple in the capacitor and considering voltage drops from the switches the calculated, the maximum capacitor voltage will likely not exceed the saturation voltage of the ADuM3190.

<table>
<thead>
<tr>
<th>( U_C ) [V]</th>
<th>( R2 ) [MΩ]</th>
<th>Standard Value</th>
<th>Note</th>
</tr>
</thead>
<tbody>
<tr>
<td>9</td>
<td>3.3</td>
<td>3.3</td>
<td>9V Battery</td>
</tr>
<tr>
<td>20</td>
<td>1.24</td>
<td>1.2</td>
<td>20V/SM Arm Test</td>
</tr>
<tr>
<td>41.7</td>
<td>0.556</td>
<td>0.56</td>
<td>( V_{DC}=250V, N=6 )</td>
</tr>
<tr>
<td>50</td>
<td>0.459</td>
<td>0.43</td>
<td>( V_{DC}=250V, N=5 )</td>
</tr>
<tr>
<td>62.5</td>
<td>0.363</td>
<td>0.36</td>
<td>( V_{DC}=250V, N=4 )</td>
</tr>
<tr>
<td>83.3</td>
<td>0.27</td>
<td>0.27</td>
<td>( V_{DC}=250V, N=3 )</td>
</tr>
</tbody>
</table>

Each resistor was measured before it was soldered into the PCB to ensure accuracy. Inaccuracies in the resistive divider result in inaccuracies in the voltage measured. Since the balancing algorithm only compares voltages a rescaling back to the capacitor’s actual
voltage is not required. The capacitors are sorted in either ascending or descending order and the sub-modules are inserted as the highest or lowest as mentioned in 4.3. The disarrangement of two or more sub-modules due to small resistive divider errors will not significantly affect the balancing as those values would have had to have been similar in the first place.

4.4.2 Analog-Digital Converter

The microcontroller first converts the voltages from analog values to digital by using an analog-digital converter (ADC). The purpose of implementing an external ADC rather than to use the built-in ADC of the microcontroller is to achieve the best precision while not sacrificing computational time requirements.

Our microcontroller features 16 port pins to convert analog inputs into digital representations, but unfortunately, only 10 were available through the Pmod connectors. Adding additional SMs for future provisions will require a new design if these inputs were used. In addition, the built-in ADC of the microcontroller is a 10-bit converter, meaning that the analog signal can be converted to one of \(2^{10} = 1024\) discrete values, ranging from ground (‘0’) to the supply voltage (‘1024’). In comparison, the AD7476 is a 12-bit converter that is capable of providing four times the precision of the built-in ADC. Precision is required to balance the SM capacitor voltages properly; they will be ideally very close to one another, and to garner the best response in our output waveform, a precise control system is required. The AD7476 was designed such that the digital representation of the analog input is to be read serially through a single pin of the microcontroller. This feature will allow us to conserve more of the port pins of the microcontroller for other uses.

The AD7476 requires two digital control signals to operate, and both will be controlled by the microcontroller. Before the conversion process can begin, the ADC starts processing the input voltage once the chip select, ‘CS’, enables the chip. This microcontroller accom-
plishes this by bringing this pin to a logic-low state. The ADC will then output the first bit on the output data line, 'SData'. The second control pin, 'SClk', is a pulsating signal from the microcontroller that determines when the ADC will output the next bit on the data line. Even though it is only a 12-bit converter, the manufacturer designed this chip requiring 16 pulses of the signal to complete the conversion. The first four bits, if read, will be zero. The following 12 will be the digital representation of the input voltage, starting with the most significant bit, and ending with the least significant bit.

This project features two functions to operate the ADC: one will initialize the port pins of the microcontroller connected to the ADC as either input or output, and the other will perform the necessary operations to read a voltage from the ADC. These two functions are displayed respectively in sections ?? and ?? of the appendix.

4.4.3 Multiplexer

Our microcontroller needs to read one voltage for every SM our converter contains. Thus, instead of implementing 10 ADCs, we will use a multiplexer to pass one voltage at a time to a single ADC.

The multiplexer (MUX) used for this project is the 16x1 CD4067B MUX. It features 16 analog inputs that can be routed one at a time to a common output pin by controlling the status of 5 digital inputs ('A', 'B', 'C', 'D' and 'INHIBIT')?. The pins labelled 'A', 'B', 'C', and 'D' are controlled by the microcontroller, and they determine which one of the inputs will appear at the output of the MUX. Since these pins can be set as either high or low, there are 16 total combinations, and each combination refers to a unique input. The purpose of the pin labelled 'INHIBIT' is to disable the MUX, and have none of the input voltages appear at the output of the MUX.

As mentioned, our microcontroller needs to process 10 total voltages from the converter. Therefore, our MUX must consist of at least 10 inputs, which we will be able to achieve
using the CD4067B. The unused inputs are grounded to prevent interference from floating voltages. The ‘INHIBIT’ pin is tied to ground to keep the MUX operational at all times, and will not be controlled by the microcontroller. The upper SM capacitor voltages are tied to the first 5 input of the MUX, and the lower SM capacitor voltages will be tied to the following 5 input pins.

One of the two functions required to operate the MUX are to initialize the port pins of the microcontroller connected to the chip. The second function changes the control signals of the MUX accordingly by an input variable to relay one of the input voltages to the output. These functions are highlighted in section ?? of the appendix.

4.5 Current Direction Measurement System

The current direction of both the upper and lower arms of the converter must be known at all times for proper balancing of the sub-module capacitor voltages. Depending on the direction of the current the sub-module capacitor can either be charging or discharging and they are inserted to reduce the voltage changes mentioned in 4.3.

The current direction is determined by using two anti-parallel diodes. This method was chosen because the voltage drop across diodes changes relatively small for a wide range of input current compared to other methods investigated such as using a Hall effect sensor or series resistor. The diodes used for the current direction measurement are the NXP semiconductor PMEG3030EP Schottkey diodes [24] rated for 3A continuous and result in a maximum forward voltage of 360mV. One disadvantage of using anti-parallel diodes is that the diode may not conduct for small amounts of arm current. The simulation case shown in figure 3.5 demonstrates that the nonconducting diodes for small arm currents do not be adversely affect the output. Figure 4.5 shows the schematic for the current measurement system.
The voltage drop across the diodes follows the polarity of the instantaneous current and passes the signal through an isolation amplifier. The AMC1100 [25] was chosen for isolation as it can operate properly with a negative common-mode input voltage while using a single ended supply. The AMC1100 can operate with a \(-160\text{mV}\) common-mode input with a differential input between \(\pm 250\text{mV}\) [25]. A resistive divider scales the voltage drop from the diodes in half to satisfy the input range and simultaneously limit the input current. A 12V supply common with the gate driver circuitry supplies a 12V-5V DC/DC converter with its output reference tied to one end of the diodes, and the 5V output tied the AMC1100. The AMC provides full isolation from the arm current and voltage and sends an output voltage with a gain of 8 directly to a comparator. The comparator chosen was the LMV331 [26] as it is compatible with 3.3V that supplies the control system and output end of the AMC1100. The comparator outputs 3.3V to the microcontroller if the isolation amplifier output is positive and 0 if it is negative which corresponds to the direction of current.
4.6 User Interface

4.6.1 Keypad

In order for the user to interface with our converter, the design contains a keypad for the user to make the required changes.

The keypad used in this project is the PmodKYPD. This keypad features 16 buttons in a 4x4 pattern, and features the numbers 0 through 9 and the letters A through F. It has 4 outputs and 4 inputs that are used to determine which key, if any, is being pressed. The outputs of the keypad are pins that are connected electronically to each row, and the inputs to the keypad are connected electronically to each column[27]. To check which key the user is pressing, the microcontroller brings the pins connected to the columns low one at a time and the microcontroller reads the pins connected to the rows of the keypad. If one of the row pins is read as low, then the corresponding column and row is mapped back to the specific key pressed.

One of the more simple components in the project, the microcontroller first needs to initialize the port pins connected to the keypad as either outputs (for columns) or inputs (for rows). A second function will poll each of the combinations of columns and rows to determine which, that is if, a key is being pressed. These two functions are shown in ?? of the appendix.

The user interface makes provision for the user to control both the modulation index of the reference waveform to limit the output voltage magnitude to a desired value, as well as the frequency of the output voltage waveform. The output frequency is restricted to be between 50 and 60Hz, which are within the typical range of frequencies used in power systems. The internal capacitors and inductors of the converter have been designed for these frequencies. If other frequencies are used, the circuit may resonate, resulting in large currents that could damage the converter.
4.6.2 Liquid Crystal Display

In addition to the keypad, a liquid crystal display (LCD) adds visual confirmation and instructions for user interfacing. It displays the present modulation index and frequency of the output voltage, as well as the keys the user may press to change either parameter.

The LCD used for this project is the PmodCLP, which contains 2 lines capable of producing 16 characters, each with a size of 5x8 pixels. Each pixel of an LCD consists of a series of liquid crystal molecules sandwiched between two filters that have perpendicular polarization.[28]. The crystals bend the incident light so that it is polarized in the same direction at the surface of each filter, allowing light to pass through[29]. By applying an electric field, or voltage, the crystals will reorientate themselves in the same direction, blocking light from transmitting through them.

The PmodCLP uses parallel data transfer with 8 data lines that can be used to both write and read from the LCD. This LCD also contains three control inputs. The register select bit, RS, determines if the data bus is connected to the internal data display register of the LCD, or the instruction register. The bit ‘R/W’ determines the direction the data bus (with respect to the microcontroller) is set to: either as output to write to the LCD, or input to read from the LCD; and ‘E’, which is an enable pin. A signal from the LCD, generally called the 'busy flag', must be cleared before anything can be written to the LCD, and is only cleared internally by the LCD. The microcontroller can write two distinct bytes to the LCD, and the first must always be an instruction. The LCD contains a pre-determined list of possible instructions[29], including clearing the display, changing the display settings, as well as writing a character to the LCD. The second byte that can be written, if necessary, is the digital representation of the character that is to be displayed on the LCD. Both of these distinct bytes are stored in internal registers of the LCD. To connect the data bus to the instruction register, the microcontroller sets the control bit ‘RS’ low, and to connect the data bus to the data register, the control bit ‘RS’ is set high. To read a byte from
the LCD, the control bit 'R/W' is set high; to write a byte, it is set low. The control pin 'E' determines when the data bus in physically connected to the internal registers of the LCD. In read mode, this pin must be set high in order to read the proper byte; otherwise, the data received will be incorrect. In write mode, the required byte must be present on the data bus first, and the byte is locked into the LCD at the instant when the pin 'E' is brought from logic high to low.

The LCD is a rather complicated component, and several functions are required to operate it. A brief list of the functions is shown here, and section ?? shows all of their respective flow charts.

- Configure port pins connected to control signals
- Configure data bus lines as either input or output, depending on whether a read or write is required
- Read a byte from the LCD
- Write a byte to the LCD
- Reading the status of the 'busy flag'
- Waiting for the busy flag to be disabled internally by the LCD
- Writing a command to the LCD
- Writing a character to be displayed on the LCD
- Changing the display settings of the LCD (with cursor, no cursor, blinking cursor)
- Clearing the LCD display
- Returning cursor to top-left corner of display
- Initializing the internal components of the LCD
Delay functions that are required when a specific minimum time of delay is required before another operation can be done with the LCD

A 4x4 keypad and a 16x2 character LCD are used to allow the user alter the operational parameters of the converter as well as visualize the change. Upon completion of the converters initialization, the LCD will display the initial values for the modulation index and frequency of the reference waveform. During this time, the user can press 'A' on the keypad to change the modulation index, 'B' to change the output frequency, or 'C' to reset the modulation index and frequency to their default values of 100% and 60Hz respectively. These instructions will also be displayed on the LCD. Once the user has pressed 'A' or 'B', the LCD will switch to display what parameter the user has selected, as well as the associated ranges for the parameter. The user will then be able to input any number using the keypad, and will be updated on the LCD in real time. The keypad does not feature a decimal point, so the frequencies that can be entered can only be whole numbers, and the modulation index must be entered as a whole number percentage. At any point, the user can press 'D' to cancel the request, and return to the default LCD display without changing either parameter. To submit the new value, the user will need to press 'C' on the keypad after entering the desired value(s). The microcontroller will then verify if the parameter entered is within the acceptable range of values. The microcontroller will update the respective parameter inside the reference waveform algorithm if it is within range, and will display a message on the LCD indicating that the parameter has been successfully changed. However, if the value is out of the range, a message on the LCD will indicate that the microcontroller has failed to register the input parameter. In either case, the LCD will go back to displaying the modulation index and the frequency, as well as the instructions to change the parameters.
4.7 Starting Routine

It is expected that the charge on each capacitor is near zero when the converter is first initialized. Hence, to avoid short circuiting the DC source, it is required that sufficient charge is on the capacitors before the DC source is connected in isolation with the capacitors. To do this, the capacitors have to be slowly charged while systematically inserting/bypassing SMs.

To implement this, it was initially decided that the capacitors will be charged via a current limiting resistor connected in series with the capacitors and the DC source. After sufficient charge can be maintained on the capacitors, the current limiting resistor will then be eliminated from the circuit with the help of a solid state relay that will then connect the DC source in isolation with the capacitors. The resistor has to be removed to limit ohmic losses within the converter. This method of charging the capacitors was unfortunately deemed not to be feasible because of the budget restrictions of the project. The monetary cost of the current limiting resistor rated to dissipate the amount of power generated by the DC source was not within the budget of the project. Also, a solid state relay able to withstand at least 500V (for safety) was required and the cost was also outside the budget.

As an alternative, it was decided that the capacitors will be charged via a rotary switch regulated voltage source. This means that the DC voltage can be slowly increased to the required DC-link voltage to charge the voltage across each capacitor.

To achieve voltage balance, while the capacitors are being charged, the SMs have to be systematically inserted/bypassed as mentioned previously. This is done with the help of a microcontroller. Since 5 SMs have to be inserted at all times during normal operation, the microcontroller sends firing pulses to the lower arm of the converter and inserts all 5 SMs in that arm. The microcontroller then bypasses the SM farthest from the alternating midpoint in the lower arm and then inserts the SM closest to the alternating midpoint in the upper arm. It does this until all 5 SMs are inserted in the upper arm. The process is
then reversed until there are only 3 SMs inserted in the upper arm and only 2 SMs inserted in the lower arm of the converter. Please note that with this operation, zero voltage cannot be achieved at the midpoint because of the odd amount of SMs on in one arm at each time. Figure 4.6 shows a diagrammatic representation of the process described.

![Diagram showing firing pulses](image)

**Fig. 4.6:** Firing pulses generated for upper and lower arms during start-up

### 4.8 Capacitor Discharge System

The capacitor discharge system is used to remove any residual charge on the capacitors when the converter is not in use. The discharge system was added as an auxiliary feature
of the converter to reduce the chance of accidental electrical shock. The schematic for the discharge system is shown in figure 4.7.

![Capacitor discharge system schematic](image)

**Fig. 4.7: Capacitor discharge system**

A power dissipation resistor is connected in series with the sub-module capacitor, a light-emitting diode (LED) indicator, and a normally closed solid-state relay. If the 12V gate driver supply is connected to a sub-module, the voltage regulator outputs 5V and current is drawn by the solid-state relay. The solid state relay will open and deactivate the capacitor discharge system with sufficient input current. If the gate-driver supply is disconnected, then there is no charge available for the solid state relay to open and the discharge system is activated. As current flows from the capacitor to the power dissipation resistor the LED will light. An input current limiting resistor of 390Ω was chosen to provide sufficient input current during converter operation.

The solid-state relay chosen was the LH1511 [30] and is rated for a load voltage of
200V and 300mA. The LH1511 was chosen as it meets our required voltage ratings and was more affordable compared to solid-state relays with higher current ratings. The project was initially intended to use a 340V dc-link with a minimum of 4 sub-modules. The maximum capacitor voltage with a 5% safety factor would then be 89.25V. A power dissipation resistor of 300Ω was chosen to limit the discharge current to 297.5mA. The required power rating of the resistor would then be

\[
P_{\text{diss}} = \frac{V^2}{R_{\text{diss}}} = \frac{89.25^2}{300} = 26.55\text{W}
\] (4.13)

The capacitor voltage will decreases quickly as it is discharged and therefore the resistor does not need to be rated for continuous 26.55W power dissipation. Resistors with 10W power ratings were chosen because they were readily available through the ECE Tech Shop.

4.9 Printed Circuit Board Design and Fabrication

A printed circuit board (PCB) ensures that each of the converter components will have a uniform layout that facilitates troubleshooting and easy assembly. The converter consists of four different PCB designs that were based on component voltage levels and functional role. The PCBs were designed using a two layer process that simplified the layout and enabled the boards to be manufactured at the University of Manitoba by the ECE staff. The PCB designs were split into the following components; sub-module, data distribution, dc-link and current direction measurement. Each PCB layout is provided in section A of the appendix. First general PCB layout design considerations are discussed followed by a description of each of the PCB designs.
4.9.1 General PCB Considerations

The minimum current carrying capability of an external PCB trace is determined by the trace thickness and width. The thickness of the PCB is determined by the rating of the copper used for the board and cannot be changed. A 1oz copper rating with a thickness of 1.4mil was used for the PCB designs. The trace width was determined from the curves in section 6.2 of [31].

Decoupling capacitors were placed as close as possible to all ICs. Decoupling capacitors provide a source of charge to smooth out the voltage for short durations and provide a path to ground for unwanted high frequency noise. Parasitic inductance must be kept to a minimum to increase the effectiveness of the decoupling capacitor. Having the capacitor as close to the IC as possible reduces the lead length and therefore causes a reduction in the parasitic inductance [32].

4.9.2 Sub-Module PCB

The sub-module PCB consists of low voltage and high voltage sections. The low voltage section comprises the components required to fire the sub-module switches and to measure capacitor voltage. These components include the optocoupler, gate driver IC and voltage measurement system. The high voltage section includes the sub-module capacitor and the switches. To provide more noise immunity the the control and measurement PCB traces were physically kept apart from the high voltage signals. Figure A.1 shows a diagram of the sub-module PCB layout.

4.9.3 Data Distribution PCB

The data distribution PCB links the control system to each submodule. The voltage measurement signals as well as firing pulses are routed from this board to the microcontroller and to each sub-module PCB. The data distribution PCB contains the MUX, ADC and the
dead-time generator circuitry. Figure A.2 shows a diagram of the data distribution PCB layout.

### 4.9.4 DC-Link PCB

The DC link PCB is the interconnection between the incoming DC voltage, the two converter arms and the outgoing AC. The DC link board holds all the high voltage and current connections, therefore the traces on this board had to be large enough to handle the large current. The DC link contains all the high voltage components such as the DC side capacitors, arm inductors and anti parallel diodes used for the current measurement system. Figure A.3 shows a diagram of the DC link PCB layout.

### 4.9.5 Current Direction Measurement PCB

The current measurement PCB connects the signals from the upper and lower arm current direction detection circuit and the microcontroller. The components of the current measurement system were placed on a separate board than that of the anti parallel diodes in order to provide maximum separation between the high voltage and the control signals. Figure A.4 shows a diagram of the data distribution PCB layout.

### 4.9.6 PCB Fabrication

The PCB design process required several iterations. This was possible because of the fact that the manufacturing was done at the University of Manitoba. During some of the earlier designs some components were too close to each other and the trace position was not optimal. During the manufacturing process some additional errors caused a set-back with the project progress. Initially there was a problem with the holes of the switches being too large during manufacturing. There was also problems with the milling machine not making the cuts deep enough causing some traces to be connected the copper planes. The problems
were eventually rectified through several productions.
Chapter 5

System Integration Testing

The purpose of system integration testing is to verify that each of the converter sub-systems are able to operate as interconnected systems. Each sub-system was individually tested to confirm that it operated as expected. The system integration testing was completed by slowly increasing the number of subsystems and the applied voltage level used for testing.

5.1 Gate Driver Testing

First, the gate driver components were tested on a breadboard as single mock sub-module. Three sub-module prototypes were then built as a proof of concept to confirm the operation of the bootstrap circuit with floating SM reference potentials. Firing pulses were generated using a signal generator and 9V batteries were used in place of SM capacitors. Figure 5.1 show the output waveform for the three sub-module prototype test.
5.2 Microcontroller Testing

Upon completion of the breadboard prototype, the PCB fabrication of the gate driver circuit was complete. The reference and modulation control using NLC was tested to verify that the proper firing signals were generated. Upon verification of NLC, the LSC-PWM control system was ready for design and implementation. Figure 5.2 shows the outputs from a four sub-module LSC-PWM control scheme without sub-module sorting.
5.3 Current Direction Measurement Testing

The PCB current direction measurement test results from a PCB are presented in figure 5.3.
The input shown as a yellow sine wave was created with a signal generator and connected to upper and lower current measurement connectors in opposite polarities to simulate a voltage drop across the diodes. The blue square wave shows the output with it’s measurement connectors in the same polarity with the signal generator. The pink square wave shows the output with it’s measurement connectors opposite polarity with the signal generator and therefore outputs the complement of the blue wave. The current direction measurement PCB works as expected.

5.4 Converter Arm Testing

First, a converter valve comprising of three PCB implemented sub-modules was assembled and tested. A picture of the cascaded sub-modules in their wood housing is shown below.
The output of the converter valve was connected to a Lab-Volt resistor bank and the sub-module capacitors where charged using the Lab-Volt DC variable source. The firing pulses were generated from the microcontroller and sent to the sub-modules via the data distribution PCB. The voltage measurements were also taken from each of the sub-modules and fed back to the microcontroller for use in the voltage sorting and balancing algorithms. The goals of this test was to verify that the control system would be able to send the correct firing pulses to the sub-modules. 67V was applied through the Lab-Volt source to charge the capacitors. The results from the voltage measurement system are shown in table 5.1.

The voltage divider uses $R_1 = 9.1\,M\Omega$ and $R_2 = 330\,k\Omega$

<table>
<thead>
<tr>
<th>Sub-Module</th>
<th>1</th>
<th>2</th>
<th>3</th>
</tr>
</thead>
<tbody>
<tr>
<td>$U_C$ [V]</td>
<td>22</td>
<td>21.6</td>
<td>22.6</td>
</tr>
<tr>
<td>$V_{IN}$ [V]</td>
<td>0.676</td>
<td>0.732</td>
<td>0.832</td>
</tr>
</tbody>
</table>

Fig. 5.4: Sub-modules
There were slight errors in the voltage measurement system due to errors in the resistance in the divider. The capacitors were then discharged to a 2400Ω load and the voltage output was recorded using an oscilloscope. The output voltage for a modulation index of 1 is shown below.

**Fig. 5.5:** Converter arm test with three sub-modules and modulation index of 1

The modulation index was then changed to 0.75 and the output was recorded.

**Fig. 5.6:** Converter arm test with three sub-modules and modulation index of 0.75
These results show that the tested arm of the MMC works as expected. The LSC-PWM waveforms appear correct in terms of shape and output voltage, but the frequency needs to be adjusted by a scaling factor. The capacitor voltage measurement system works as expected and was connected to the microcontroller for voltage measurements, but the sorting and balancing algorithm could not be tested due to the unidirectional current. This section demonstrated that each sub-system works on it’s own and a majority of the sub systems have been interfaced.
Chapter 6

Future Work

The converter designed was implemented in such a way that there is sufficient room for improvement. The future considerations that can be made are in a wide range of different facets. This section outlines those improvements we feel are possible given the current design.

6.1 Switch Protection

Snubber circuits and heat sinks were not considered in the initial design because of an assumed low operating voltage and current relative to the switch’s ratings. Due to time constraints these were not added as the project progressed. Future designs of the converter should consider these protective measures.

6.2 Proposed Gate Driver Revision

Figure 6.1 shows a revised circuit for the gate driver sub-system. The changes are demonstrated with blue connection lines. The fundamental change in this circuit is that the output of the optocoupler and gate driver input is supplied from a DC/DC converter
with its output reference tied to the sub-module’s reference. The entire gate driver circuit could be supplied with a single voltage through the DC/DC converter. Furthermore, since the gate driver IC supplying the lower MOSFET has its COM pin tied to the sub-module reference a low side driver could be used instead. A dual gate driver IC featuring a low and high side driver such as the IR2110 [33] could be used to reduce the component count in circuit. The revised gate driver circuit was breadboard tested and verified to work. The proposed design was not developed on a printed circuit board however due to time and budget constraints.

Fig. 6.1: Revised gate driver design
6.2.1 Three-phase Converter

Power converters or motor drives in higher power ranges usually require three-phase equipment. The single-phase converter built can easily be improved to a three-phase converter by making three identical legs of the converter and implementing slightly different controls to account for phase-shifts between the output phases.

6.2.2 Closed-loop Converter Control

The control system of the converter can be extended to include closed loop controls. An updated control system can have a feedback system that continually measures the generated about voltage and compares it to a reference voltage and systematically adjusts the system to generate the required voltage. This can be achieved using a proportional integral (PI) controller or proportional integral derivative controller (PID). Another benefit of using a closed loop control system could be to change the pulse width duration or timing of the sub-module firing pulses to reduce circulating current and account for dead-time.
Chapter 7

Conclusions

This report outlined and discussed the various tasks and components required to build a fully functioning MMC using the cascaded Half-Bridge SM. A single-phase converter design is proposed and proven through simulation. The gate-driver circuitry, reference and modulation, capacitor voltage and current direction measurement, capacitor discharge system, capacitor voltage balancing and sorting and the production of the PCBs were all discussed in detail. The functioning role, design and implementation of each sub-system was outlined and future design considerations were proposed. The initial project specifications required the physical building and testing of an MMC prototype producing low output distortion for an output power of 100VA. All of the MMC sub-systems were tested and proven to work as individual components and the results were presented. A systematic process for integrating the MMC sub-systems was described. The test results of an MMC arm are presented and verify that the gate driver circuitry, measurement and control systems work and that a single-phase MMC prototype can be built with the existing design.

We are confident that one week from now by March 11, 2015 that two arms of the MMC prototype will be connected via arm inductors and dc-link capacitors. The current measurement system will be connected to acquire the direction of current in each arm, and
a functional MMC producing at least 4 output levels with a DC voltage of 120V will be made.
References


Appendix A

Printed Circuit Board Layouts
Fig. A.1: Sub-module PCB layout
Fig. A.2: Data distribution PCB layout
Fig. A.3: DC link PCB layout
Fig. A.4: Current measurement PCB layout
Appendix B

Budget

Table B.1 shows the total budget of the project. Parts that were received from the ECE department were not counted towards the total project budget. The project is $175.47 over of our proposed budget of $642.02, totalling $817.49. The project ran over budget due to an oversight during the project proposal of the number and types of components needed.
Table B.1: Project budget

<table>
<thead>
<tr>
<th>Part</th>
<th>Supplier</th>
<th>Cost</th>
<th>Quantity</th>
<th>Subtotal</th>
</tr>
</thead>
<tbody>
<tr>
<td>Arm Inductor (2.2mH, 4A)</td>
<td>Digikey</td>
<td>$7.65</td>
<td>2</td>
<td>$15.30</td>
</tr>
<tr>
<td>SM capacitor (6.8mF, 100V, 6.5A)</td>
<td>Digikey</td>
<td>$6.70</td>
<td>16</td>
<td>$107.20</td>
</tr>
<tr>
<td>Half-Bridge switches (IRFI4019HG-117P)</td>
<td>Digikey</td>
<td>$3.25</td>
<td>16</td>
<td>$52.02</td>
</tr>
<tr>
<td>Gate drivers (IR2118PBF)</td>
<td>Digikey</td>
<td>$2.14</td>
<td>32</td>
<td>$68.35</td>
</tr>
<tr>
<td>5V-15V DC-DC converter (VIBLS1-S5-S15-SIP)</td>
<td>Digikey</td>
<td>$5.78</td>
<td>16</td>
<td>$92.48</td>
</tr>
<tr>
<td>5V-5V DC-DC converter (VIBLS1-S5-S5-SIP)</td>
<td>Digikey</td>
<td>$5.78</td>
<td>2</td>
<td>$11.56</td>
</tr>
<tr>
<td>Optocoupler (H11L2M)</td>
<td>Digikey</td>
<td>$1.41</td>
<td>26</td>
<td>$36.66</td>
</tr>
<tr>
<td>Dead-time generators (IXDP630PI)</td>
<td>Digikey</td>
<td>$4.45</td>
<td>6</td>
<td>$26.70</td>
</tr>
<tr>
<td>Pmod LCD (410-142P)</td>
<td>Digikey</td>
<td>$37.99</td>
<td>1</td>
<td>$37.99</td>
</tr>
<tr>
<td>Multiplexer (CD4067BE)</td>
<td>Digikey</td>
<td>$2.99</td>
<td>2</td>
<td>$5.98</td>
</tr>
<tr>
<td>Isolation amplifier (ADUM3190A)</td>
<td>Digikey</td>
<td>$2.99</td>
<td>12</td>
<td>$35.88</td>
</tr>
<tr>
<td>Solid State Relay (LH1511BAB)</td>
<td>Digikey</td>
<td>$3.72</td>
<td>12</td>
<td>$44.64</td>
</tr>
<tr>
<td>PCB board</td>
<td>Digikey</td>
<td>$27.30</td>
<td>4</td>
<td>$109.20</td>
</tr>
<tr>
<td>2 position terminal block</td>
<td>Digikey</td>
<td>$0.56</td>
<td>17</td>
<td>$9.52</td>
</tr>
<tr>
<td>4 position terminal block</td>
<td>Digikey</td>
<td>$0.96</td>
<td>24</td>
<td>$23.04</td>
</tr>
<tr>
<td>8 position terminal block</td>
<td>Digikey</td>
<td>$2.54</td>
<td>1</td>
<td>$2.54</td>
</tr>
<tr>
<td>6 position terminal block</td>
<td>Digikey</td>
<td>$1.90</td>
<td>4</td>
<td>$7.60</td>
</tr>
<tr>
<td>12 position terminal block (small form factor)</td>
<td>Digikey</td>
<td>$3.53</td>
<td>3</td>
<td>$10.59</td>
</tr>
<tr>
<td>12 position terminal block (large form factor)</td>
<td>Digikey</td>
<td>$2.58</td>
<td>1</td>
<td>$2.58</td>
</tr>
<tr>
<td>Comparitor (LMV331DBVR)</td>
<td>Digikey</td>
<td>$0.88</td>
<td>12</td>
<td>$10.56</td>
</tr>
<tr>
<td>Differential amp (AM1100)</td>
<td>Digikey</td>
<td>$6.51</td>
<td>7</td>
<td>$45.57</td>
</tr>
<tr>
<td>12V-5V DC-DC converter (VIBLS1-S12-S5-SIP)</td>
<td>Digikey</td>
<td>$7.26</td>
<td>3</td>
<td>$21.78</td>
</tr>
<tr>
<td>Diode, Shotkey (PMEG3030EP)</td>
<td>Digikey</td>
<td>$0.57</td>
<td>8</td>
<td>$4.56</td>
</tr>
<tr>
<td>Fuse holders (Schurter Inc 3101.0045)</td>
<td>Digikey</td>
<td>$4.10</td>
<td>2</td>
<td>$8.20</td>
</tr>
<tr>
<td>Resistor (high tolerance 3.9 k)</td>
<td>ECE department</td>
<td>$0.14</td>
<td>4</td>
<td>$0</td>
</tr>
<tr>
<td>Capacitor (high tolerance 47 pF)</td>
<td>ECE department</td>
<td>$0.10</td>
<td>4</td>
<td>$0</td>
</tr>
<tr>
<td>Capacitor (ceramic 1uF)</td>
<td>ECE department</td>
<td>$0.52</td>
<td>88</td>
<td>$0</td>
</tr>
<tr>
<td>Capacitor (ceramic 10 uF)</td>
<td>ECE department</td>
<td>$0.52</td>
<td>24</td>
<td>$0</td>
</tr>
<tr>
<td>Capacitor (ceramic 0.1 uF)</td>
<td>ECE department</td>
<td>$0.52</td>
<td>24</td>
<td>$0</td>
</tr>
<tr>
<td>Regulator (5V)</td>
<td>ECE department</td>
<td>$2.14</td>
<td>12</td>
<td>$0</td>
</tr>
<tr>
<td>Resistor (200 ohm)</td>
<td>ECE department</td>
<td>$0.10</td>
<td>24</td>
<td>$0</td>
</tr>
<tr>
<td>Resistor (270 ohm)</td>
<td>ECE department</td>
<td>$0.10</td>
<td>24</td>
<td>$0</td>
</tr>
<tr>
<td>Resistor (10 ohm)</td>
<td>ECE department</td>
<td>$0.10</td>
<td>24</td>
<td>$0</td>
</tr>
<tr>
<td>Resistor (high tolerance 9.1 M ohm)</td>
<td>ECE department</td>
<td>$0.14</td>
<td>12</td>
<td>$0</td>
</tr>
<tr>
<td>Resistor (high tolerance 249 k)</td>
<td>ECE department</td>
<td>$0.14</td>
<td>12</td>
<td>$0</td>
</tr>
<tr>
<td>Resistor (3.9 k)</td>
<td>ECE department</td>
<td>$0.14</td>
<td>12</td>
<td>$0</td>
</tr>
<tr>
<td>Resistor (400 Ohm)</td>
<td>ECE department</td>
<td>$0.14</td>
<td>12</td>
<td>$0</td>
</tr>
<tr>
<td>Resistor (300 Ohm 10W)</td>
<td>ECE department</td>
<td>$0.83</td>
<td>12</td>
<td>$0</td>
</tr>
<tr>
<td>Diode</td>
<td>ECE department</td>
<td>$0.14</td>
<td>12</td>
<td>$0</td>
</tr>
<tr>
<td>LED</td>
<td>ECE department</td>
<td>$0.25</td>
<td>12</td>
<td>$0</td>
</tr>
<tr>
<td>DC-Link Capacitors</td>
<td>ECE department</td>
<td>$5.37</td>
<td>2</td>
<td>$0</td>
</tr>
<tr>
<td>ChipKITPro MX7 Board</td>
<td>ECE department</td>
<td>$100</td>
<td>2</td>
<td>$0</td>
</tr>
</tbody>
</table>

Total                                                                 $817.49
Appendix C

Second Appendix

C.1 Master Microcontroller Functions

The following functions illustrate the functions within the microcontroller responsible of user interfacing, and generation of the reference and carrier waveforms. This microcontroller outputs the number of SMs needed to be inserted in the lower arm to the secondary controller.

C.1.1 Main Function
C.1.2 Device Initialize
C.1.3 Interrupt Initialization
C.1.4 Timer2 Interrupt
C.1.5 Timer45 Interrupt
C.1.6 Handshaking Initialization
C.1.7 Handshaking Function

C.2 Slave Microcontroller Functions

C.2.1 Main Function
C.2.2 Device Initialization
C.2.3 Handshaking Initialization
Fig. C.1: This function is the main function of the master converter.
Fig. C.2: This function calls the initialization functions of the LCD, keypad, interrupts, and port pins to interface with the second controller.
Fig. C.3: This function initializes the interrupt functions used by the reference controller.
Fig. C.4: This function determines the number of SMs to be inserted in the lower arm every time the Timer2 interrupts the main function.
Fig. C.5: This function changes the display of the LCD every two seconds by interrupting the main function.
Fig. C.6: This function initializes the port pins connected to the second microcontroller.
Fig. C.7: This function initiates the communication with the second controller every time Timer2 interrupts.
Fig. C.8: This function determines the firing pulses every time the primary controller sends data to this controller
Fig. C.9: This function initiates the port pins connected to the MUX and ADC, as well as the pins that send the firing pulses.
Fig. C.10: This function initializes the port pins connected to the primary microcontroller.